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Design of High Speed and Low Area Confined Multiplier on FPGA

Kandagatla Ravi Kumar[1]; Cheeli Priyadarshini[2]; Kanakam Bhavani[3]; Ankam Varun Sundar Kumar[4]; Palanki Naga Nanda Sai[5]

[1]Associate Professor, Department of ECE, Lakireddy Bali Reddy College of Engineering, Mylavaram, India.
[1]k6ravi@gmail.com

[2]Department of ECE, Lakireddy Bali Reddy College of Engineering, Mylavaram, India.
[2]priyadarshinicheeli@gmail.com

[3]Department of ECE, Lakireddy Bali Reddy College of Engineering, Mylavaram, India.
[3]bhavani.kanakam23@gmail.com

[4]Department of ECE, Lakireddy Bali Reddy College of Engineering, Mylavaram, India.
[4]varunsundar27@gmail.com

[5]Department of ECE, Lakireddy Bali Reddy College of Engineering, Mylavaram, India.
[5]naganandasai5@gmail.com

Abstract

In this Advanced world, Technology is playing the major role. Most importantly development in Electronics field has a large impact on the improved life style. Among the advanced applications, DSP ranks first in place. Multipliers are the most basic elements that are widely used in the Digital Signal Processing (DSP) applications. Therefore, the design of the multiplier is the main factor for the performance of the device. Using RTL simulation and a Field Programmable Gate Array (FPGA), we compare the performance of a serial multiplier with an advanced multiplier. Many single bit adders are removed and replaced with multiplexers in this project. So that the less often used FPGAs are fully used by occupying fewer divisions and slices. The use of multiplier architecture results in significant reductions in FPGA resources, latency, area, and power. These multiplication approaches are created utilizing RTL simulation in Xilinx ISE simulator and synthesis in Xilinx ISE 14.7. Finally, the Spartan 3E FPGA is used to implement the design.

Key-words: FPGA, Multiplier, Xilinx, CSLA.

1. Introduction

The desire to push technology to new heights has resulted in a slew of new processes and designs that are both faster and more compact than prior technologies. As the VLSI industry moves toward more compact designs with greater performance, it becomes increasingly important to build

components that are compatible with the development. In terms of processor performance, the multiplier is a critical logic device. The processor's role is critical in every system. Multiplication is the operation that takes up the majority of the processor's time, therefore improving the multiplier's efficiency contributes to improved processor performance, notably in the fields of digital data processing ASIC and signal processing. The carry look-ahead adder and the carry save adder are used in this study to demonstrate two different types of multipliers. Following the development of these two different types of multipliers, a comparison study of the two designs area and power consumption is being conducted. As chip component sizes shrink in order to provide mobility, power dissipation becomes an issue. At its most fundamental level, multiplication may be described as the process of repeatedly adding a number to itself. As a result, that addition is a sub-process inside the multiplication criteria that must be satisfied can be ignored. The final result was created using fast adders after the partial products were aligned in the shape of a tree. The final phase is FPGA implementation, which comes after the architectural design and comparison.

The dynamic voltage level shifter has capability to shift low voltage to high voltage with a provision of data blocking, designed with abnormal aspect ratios. It is the major disadvantage to all digital circuits like Adders, Multipliers and Embedded processors [7].

The basic computing mechanism in multi core processors is interconnecting multiple cores to exchange the data between multiple cores. It utilizes voltage level shifters to interface multiple cores, have designed with wide width transistors leads to abnormal aspect ratios [8].

The level shifter which have designed using transmission gates may be good in passing logic ‘1’ but the power consumption is huge while passing ‘0’. This kind of level shifters more appropriate for threshold voltage level shifting and lagging in sub or deep threshold voltages, It could the major drawback for digital circuits like arithmetic operations of Embedded processors [9].

The level shifters which have designed using cascaded transistors are efficient at power consumption but the propagation delay is huge. This kind of level shifters are more appropriate for near threshold voltage computations and lagging at deep threshold voltages computations, It could the major drawback for digital circuits [10].

M. Mahaboob Basha and Towfeeq Fairooz et al, performed LFSR counter analysis using CMOS sub-micrometer, so as to attain smaller chip size with lofty operating speeds and efficient usage of energy. From the results it is clear that the LFSR counter has additional benefits when compared to other counter parts, therefore it is a new trend setter in the field of communication for computing applications [7].

In the field of communication, energy efficient computing will play a vital role to maximize the circuit performance when we operate the device at sub threshold or near threshold regime. The effective solution to minimize the energy consumption of a circuit is MTCMOS at low power applications and GLBB is at ultra low power applications [8].

The results show that the proposed design achieves very good performance in terms of power and delay. The change detection and background removal application can be also realized by division operation. In image analysis, if only integer division is performed, then the results are typically rounded at the output to the next lowest integer. Restoring array dividers is used to compute the same 8-bit grayscale images. Case study for image processing also shows the validity of the proposed designs [9].

Adder

Adder is a functional block that is used to add two numbers together. In this article, the adders that will be examined are binary adders that only add binary integers. The two most common adders are the full adder and the half adder. These simple adders are required to create more sophisticated Carry Select Adders.

Carry Select Adder

The adder is traditionally divided into blocks when using the carry choose addition method. If the adder is an n-bit adder, and we wish to divide it into blocks of m bits each, the number of blocks generated is obviously n/m blocks. To create the output sum and carry signals, these n/m blocks execute addition of m-bits using any of the adder algorithms such as ripple carry adder, carry save adder, carry look-ahead adder, and so on. n/m blocks in the CSLA may now be regarded as n/m stages, each consisting of two m-bit adders and one m-bit 2-to-1 multiplexer, with the exception of the initial stage block, which includes the least significant bits of the two. The subsequent blocks repeat the addition twice, one with a carry-in of 1 and the other with a carry-in of 0. The right pair is retrieved when the real carry-in value becomes accessible, and these pre-calculated sum bit values with their corresponding pre-assumed carry-in values are stored in the block. With the aid of a 2-to-1 MUX, the work of selecting the appropriate pair is now accomplished. The MUX's select line is made up of the actual carrying signal.

Multiplier

A multiplier is a device that multiplies two numbers. In the multiplication process, each bit of the multiplier is multiplied by each bit of the multiplicand, yielding partial products. These incomplete components are then combined to create the final result. Array multipliers and tree multipliers are the two primary forms of multipliers.

2. Literature Survey

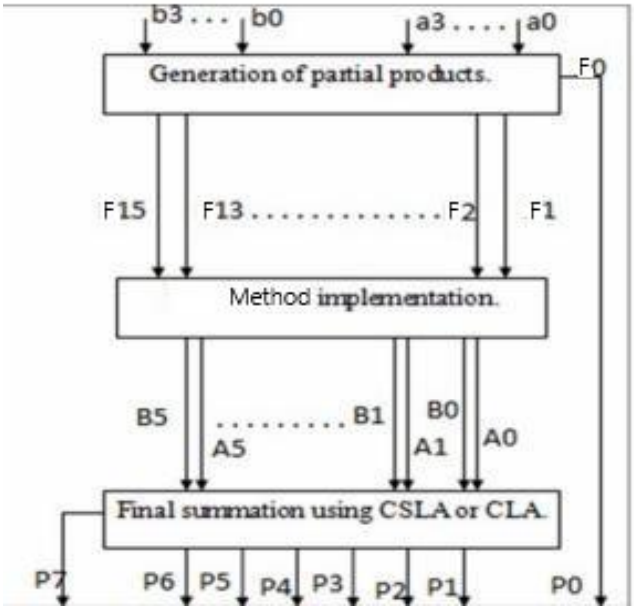
VLSI circuit designers are majorly concerned with integrated circuit power dissipation. A multiplier is a fundamental hardware component in most of the digital and high-performance systems, such as digital signal processors, FIR filters and microprocessors. Most significant multipliers for digital technologies are specific product development and reductions. Using the Full adders approach, we may remove incomplete products and increase application time. Further improvement of these techniques will minimize power consumption and increase speed, resulting in higher accuracy. Previous papers proposed the design of multipliers but all the methods are beneficial for only the few bit numbers. But large bit numbers oriented applications are not capable to apply those methodologies so here we design a multiplier which has high speed, less area and maximum accuracy. For this design we are in need of half adders, full adders and multiplexers in order to reduce the area occupied by the gates.

3. Proposed Methodology

The study described in this dissertation paper offered two alternative designs for the multiplier. In one design, multiplier is combined with a carry choose adder, whereas in the other, it is combined with a carry look-ahead adder. Then there's a comparison study in terms of area and electricity usage. Then there's a comparison study in terms of area and electricity usage. The physical implementation of the suggested architecture is the thesis's final goal. The implementation of the hardware is the programming in VHDL is developed in MODELSIM on the FPGA Spartan 3e device with Xilinx atmosphere. The three key phases in the thesis methodology are:

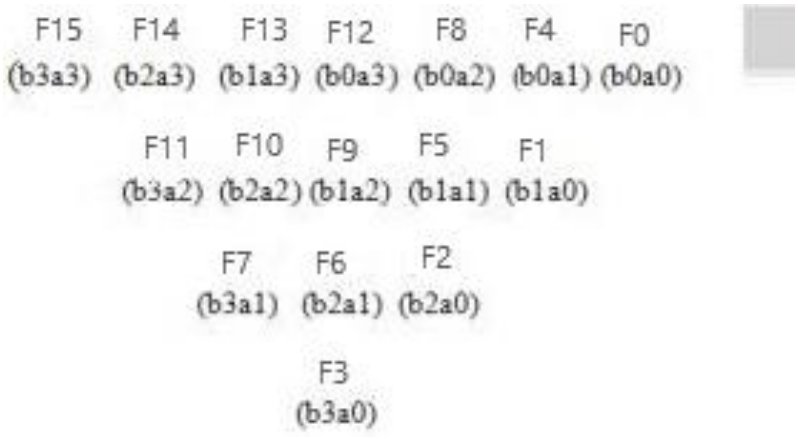
- Generation of partial products.
- Implementing the multiplier using partial products and half and full adders.
- Using the Carry select adder as a final conclusion (CSLA).

Fig. (a) - Design Flow of Proposed Work



When the suggested architectures are properly constructed, we can determine the area and power consumption with the assistance of the mapping report and compare which architecture gives the best results. In this approach, the partial products having same weights are combined together and kept in a column. Based on the greatest weight carried by partial product terms, the arrangement is split into six columns, with a3b3 having the largest weight 6. Half and full adders are now used to add the numbers in each column, depending on the scenario, a half adder is used for adding the two numbers and a full adder is used for adding three numbers. The main objective of the Wallace tree implementation in this design is to implement input terms for CSLA adders. The initial partial product a0b0, as we know, does not require any computation and is regarded as the product's LSB. R0 equals P0 as a result.

Fig. (b) - Partial Products Formation



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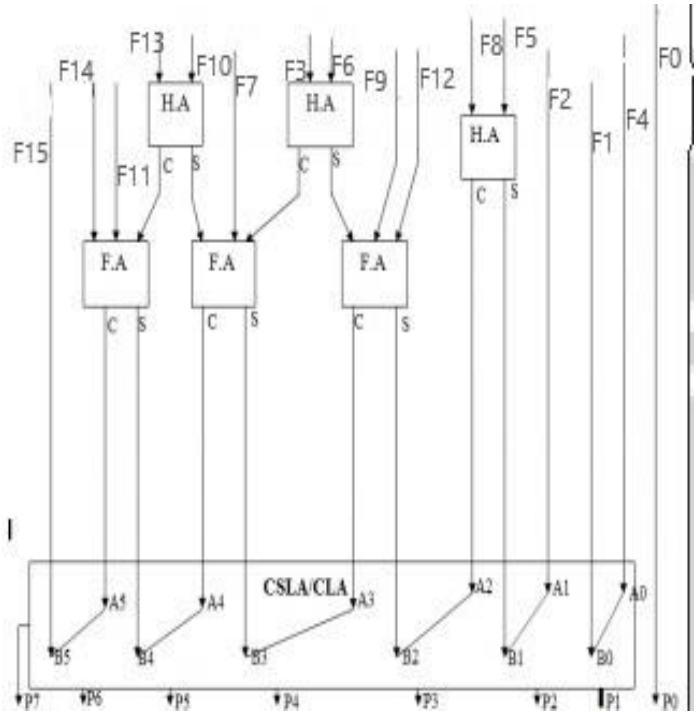
The purpose now is to bring out two last bits from each of the remaining columns after deletion of the first column from the right since it contains F0. When we look closely to the columns, we can detect that the second column from the right includes two partial products, P4 and P1, implying that only has two bits in total and may be referred to as A0 and B0. We have three words in the next column: P2, P8, and P5, therefore we'll require using the adders to get the last two bits for CSLA. Half adder provides two outputs: sum and carry, when p8 and P5 are used as inputs. B1 is the total obtained, A1 is the partial product term P2, and carry received from this column is A2. If we keep going in this direction, we'll get A0B0, A1B1, A2B2, A3B3, A4B4, and A5B5. These figures can now utilized for adding two input numbers. The figure below depicts the adder stage as well as the multiplier implementation.

Fig (c) - Multiplier using CSLA



The adding of the bits received is the final step after the multiplier implementation. We get a total of 12 bits from the Wallace tree computing process, which may be split into two numbers: A(A0, A1, A2, A3, A4, A5) and B (A0, A1, A2, A3, A4, A5) (B0, B1, B2, B3, B4, B5). By combining the integers A and B, the product of the numbers (a) and (b) may now be found. The product's LSB, which is nothing but F0, is already known. As a result, P0 = F0. The remaining parts of the product will now be determined by adding A and B. The product bits are the sum bits at each step, and the carry passes to next stage. The MSB of the product is final carry out. As a result,

following the last step, we have p1, p2, p3, P4, p5, P6, and p7. The hardware implementation of multiplier design described in this study on FPGA Spartan 3E is the final phase of the given work. The programming is done in VHDL, and the code is burned into the FPGA kit using the Xilinx tool. The simulation is carried out in both the Xilinx and the Intel environments. FPGA implementation is used to do the area and power analysis.

4. Results

Fig. (d) - Outline of Multiplier

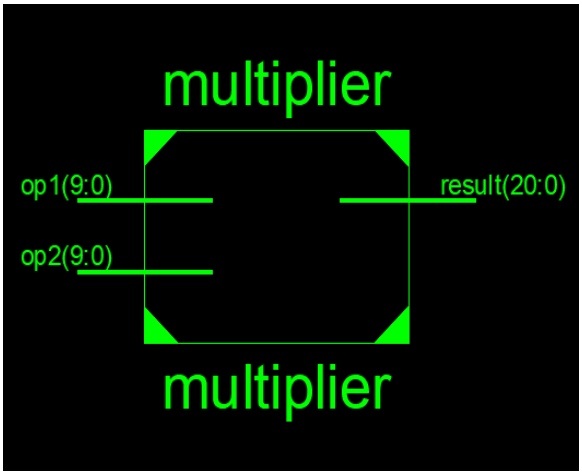


Fig. (e) - RTL Schematic of Multiplier

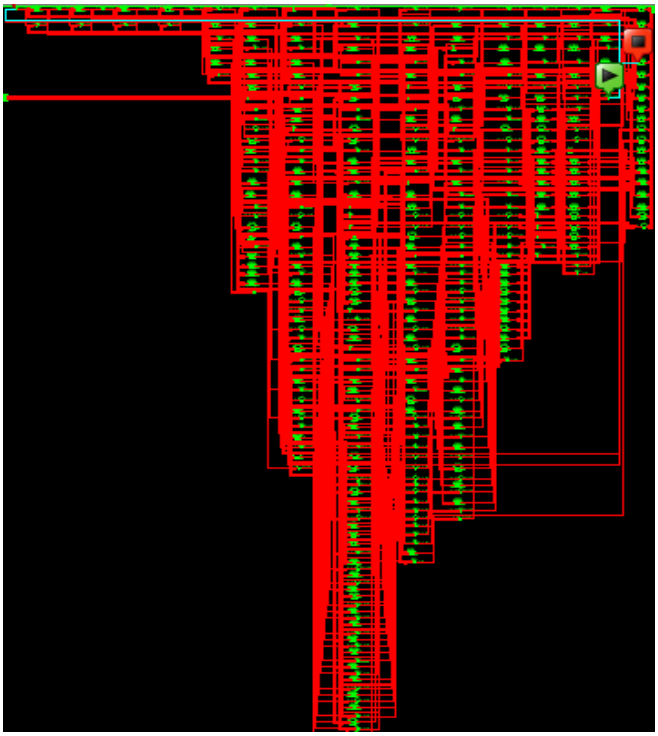


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Fig. f -Technology Schematic of Multiplier

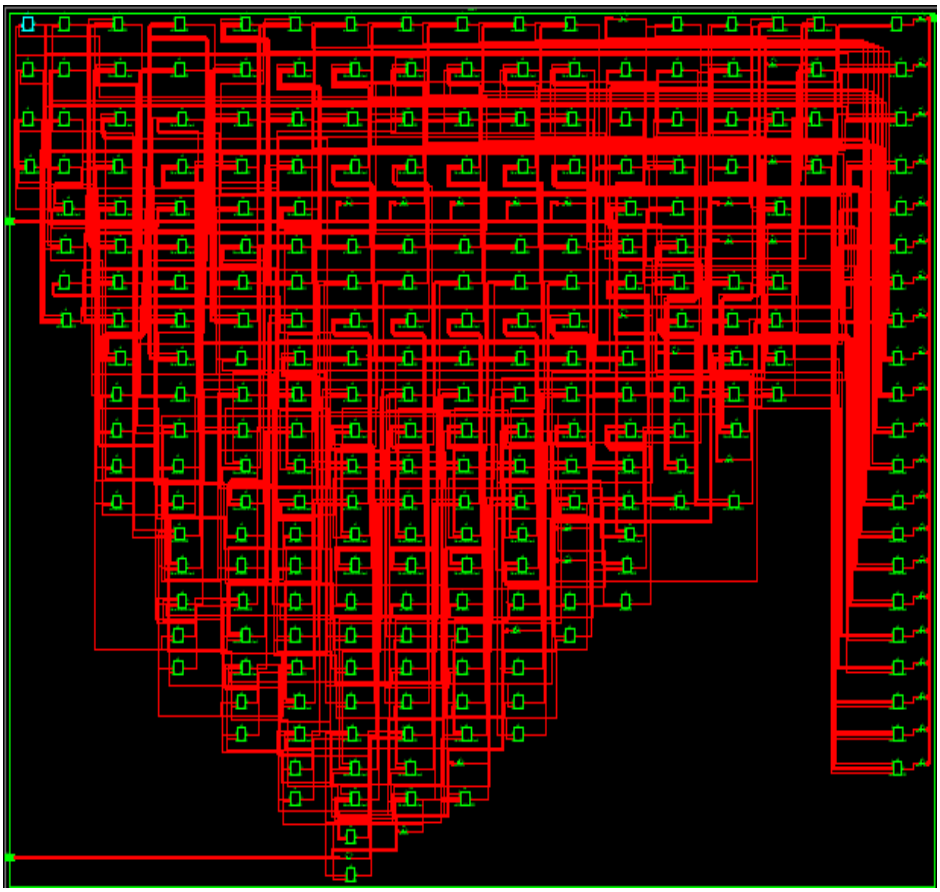
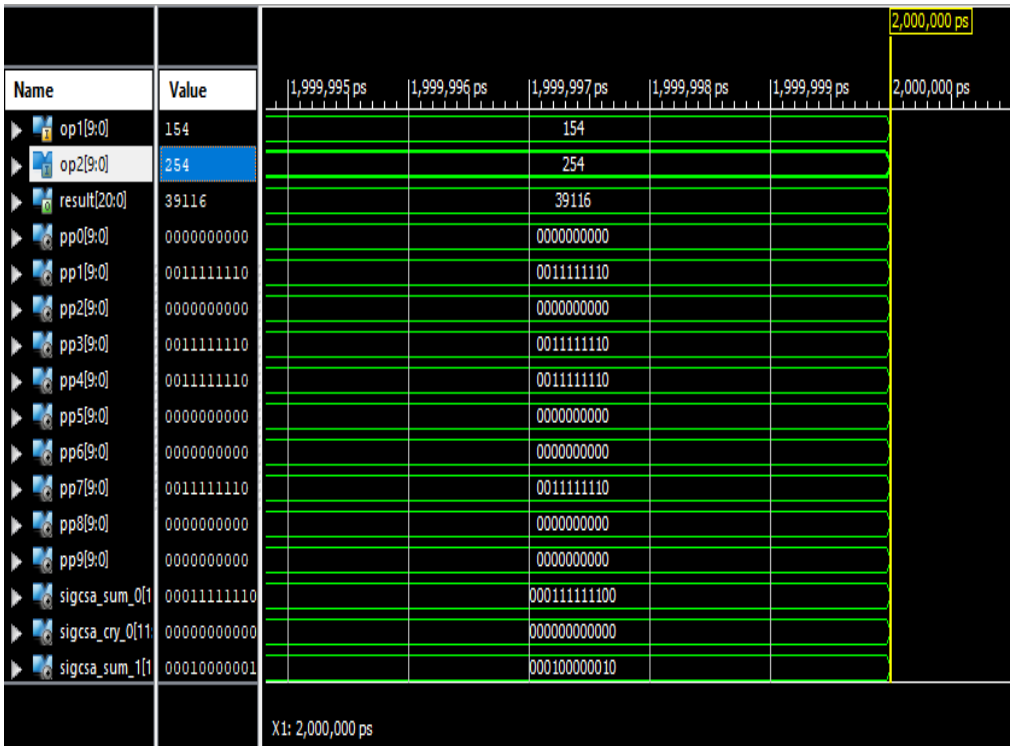


Fig. g - Simulation Result



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Parameters

Area

Device Utilization Summary				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of 4 input LUTs	249	9,312	2%	
Number of occupied Slices	139	4,656	2%	
Number of Slices containing only related logic	139	139	100%	
Number of Slices containing unrelated logic	0	139	0%	
Total Number of 4 input LUTs	249	9,312	2%	
Number of bonded IOBs	41	232	17%	
Average Fanout of Non-Clock Nets	3.05			

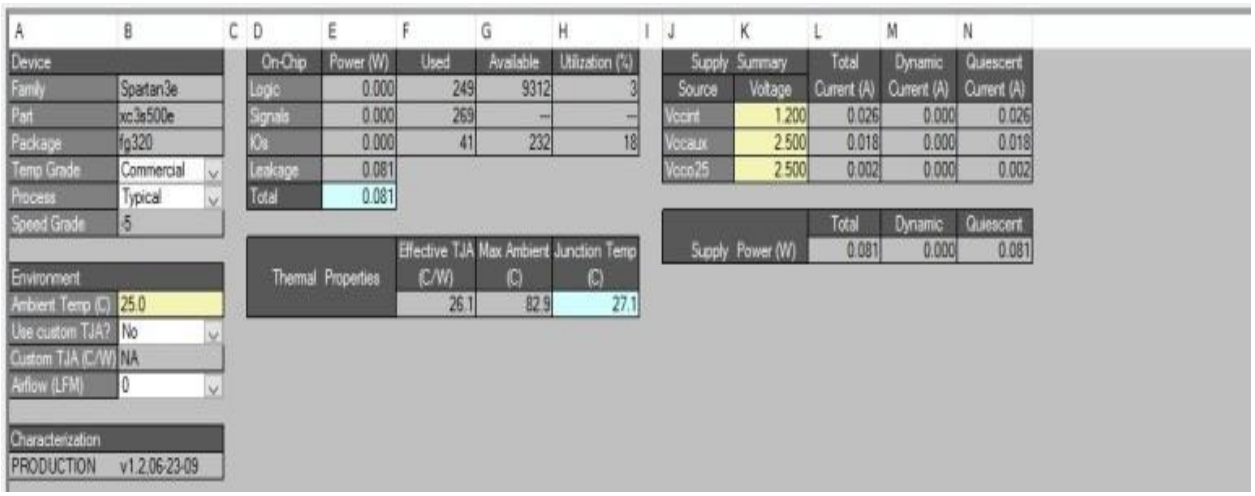
Delay

```
    ----------------------------------------
    Total                     24.773ns (15.291ns logic, 9.482ns route)
                                       (61.7% logic, 38.3% route)

=========================================================================


Total REAL time to Xst completion: 30.00 secs
Total CPU time to Xst completion: 29.49 secs
```

Power



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5. Conclusion

Based on the area and power consumption of the multiplier designs proposed in this article, it is clear that the multiplier with carry select adder is superior in terms of both area and power consumption, as shown in the comparative tables. Several forms of multiplier designs are investigated and compared to the traditional multiplier architecture in this study. Multiplier design is found to perform better in terms of power, latency, and area when the complexity is decreased and efficient adders are used.

6. Future Scope

Multipliers are without a doubt the processors backbone, particularly in digital signal processing. We can now see the scope and execution of the Digital Multipliers, particularly the Wallace tree multiplier, because we have gone through the full thesis. The thesis covers all of the important aspects of the design, including adders (both conventional and fast adders) and multipliers (all varieties). This lays the foundation for our theory and makes it easier to comprehend. The desire to build better and more efficient multiplier architectures has steered multiplier development toward more lucrative designs. This thesis proposes a design that takes into account all of the technological restrictions that exist today. The primary focus is on creating a design that is hardware implementable and uses less space and power. Because space and power are two of the most pressing demands for future designs, they must be examined and analyzed. As a result, we may conclude by examining the area and power reports to determine which design is superior to the two recommended architectures, which is the multiplier utilizing carry select adder architecture.

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