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# FPGA based Design of Triple Modular Redundancy for Hybrid Digital Pulse Width Modulation Generator

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**Abstract**

*This paper proposes the Triple Modular Redundancy checker for the Hybrid Digital Pulse Width Modulation generator to verify the correctness in the output signal. The proposed design involves replicating the Hybrid Digital Pulse Width Modulation Generator thrice and the majority voter circuit validates the correct output by considering the two accurate signals out of the three outputs. The digital pulse width modulation generator is broadly classified as Counter-based Digital Pulse Width Modulation, Delay line-based Digital Pulse Width Modulation, and Hybrid-based Digital Pulse Width Modulation. Among the three methods, the Hybrid based Digital Pulse Width Modulation is preferred as the Counter-based Digital Pulse Width Modulation uses high clocking frequency and the Delay line-based Digital Pulse Width Modulation occupies a large area. The proposed Triple Modular Redundancy is implemented using the FPGA and parameters such as power analysis and device utilization chart.*

**Key-words:** Triple Modular Redundancy, Digital Pulse Width Modulation, Field Programmable Gate Array.

## 1. Introduction

The faults and failures are prone to happen in any system during its operation. The faults are responsible for the malfunctioning of the components used in the system. Based on the complexity and time duration for the repair of the faults, the faults are broadly classified as Permanent and Temporary Faults.

Faults in the digital environment play a pivotal role in the performance of the circuit as they could introduce several delays in the propagation of values from the input to the output. Several methods of testing digital circuits could identify, isolate and rectify the faults by the generated Test pattern sets. But these methods are time-consuming and decrease the performance of the circuit. To overcome these, the Redundancy method is introduced that includes the replication of the circuit under test and allows the circuits to perform in parallel. The redundancy is complete only when the checker is added to validate the output from the majority error-free output from the replicated circuits.

The TMR method consists of three replications of the Circuit under Test along with the Majority voter circuit. The Triple Modular Redundancy exhibits high reliability and energy efficiency for both transient and permanent faults [1] The TMR based system provide exceptional fault identifying and correction with the evolution of heterogeneous processor in semiconductor industry [2]. The TMR without the voter circuit is used as a cost-effective and tolerant latch design that produces a high-speed transmission path, clock gating, and fewer transistors in the design [3]. The ATMR techniques use the pass transistor logic for the majority voter circuit to minimize the internal fault propagation to the output [4]. The importance of fault masking is stressed in the ATMR based design technique using the dedicated tool [5]. The STMR occupies a low area and minimum reliability loss compared to the TMR method [6].

The 90nm CMOS technology-based Quaded structure NAND gate is designed to ensure the safe operation of the majority voter block in the TMR and NMR techniques [7]. The reliability of the mission-critical system is analyzed using the co-designed fault injector to identify and withstand long-duration faults [8]. The FPGA-based TMR technique has a 30% longer lifetime than the FMR technique and also utilizes fewer devices than the modified triplex-duplex method[9]. The TMR circuit designed using the FPGA can produce up to 26 times reduction in Neutron testing than the unmitigated design [10]. The real implementation of TMR for high-speed digital circuits reduces 44% of the switching power consumption [11].

Though TMR is utilized in several digital circuits, the extension of TMR in real applications such as power converters and inverters is minimal. The fault-tolerant PWM generator utilizes the double redundant control model to assure the correct operation of the inverter gate [12]. The redundancy technique in fusion with the switches can detect, isolate, and compensate for the faulty semiconductor switch of the Inverter circuit [13]. The enhanced reliability is provided to the TMR by making use of a hybrid redundancy method to regulate the DC-DC converter circuit [14].

The proposed method analyzes the performance of the Hybrid Digital Pulse Width Modulation generation circuit using the Triple Modular Redundancy methods. The HDPWM generator is injected with the fault injector in the duty cycle input and verified with the output of the Majority Voter circuit. For the sake of validation, the proposed method is evaluated with the Artix 7 FPGA family device in the Xilinx Vivado Tool. The following section discusses the evolution of the Hybrid Digital Pulse Modulation generator, Triple Modular Redundancy, and the proposed model of TMR-based HDPWM generator along with the results.

## 2. Digital Pulse Width Modulation Generator Design

The proposed method involves the identification of the fault in the generation of the Digital Pulse Width modulation generator. The Hybrid Digital Pulse Width Modulation is considered for the evaluation fault-free operation with the utilization of Triple Modular Redundancy Checker. This section will discuss the HDPWM design followed by the TMR algorithm for the HDPWM generator.

### a) Hybrid Digital Pulse Width Modulation Generator

The Hybrid Digital Pulse Width Modulation is the combination of two DPWM algorithms namely Counter based DPWM and Delay line based DPWM. The design of HDPWM uses the 210-bit resolution in its design and bit split into two sections as 25 bits for the CDPWM and DDPWM algorithms. The CDPWM and DDPWM algorithms generate the SETs and RESETs signals and these are combined using the logical AND gate to give the SET and RESET for the HDPWM as shown in Fig.1. The working of the two algorithms namely CDPWM and DDPWM is given below.

### b) Counter Digital Pulse Width Modulation Generator

In Counter based DPWM algorithm, the counter circuit of 210 bits resolution is utilized as the asymmetric carrier wave. In this work, the UP Counter circuit is used and hence it is referred to as Leading Edge CDPWM. Similarly, based on the type of counter, the algorithm is specified as Trailing-Edge CDPWM for DOWN Counter circuit and as Triangular CDPWM for UP/DOWN counter circuit. The period for the counter is manipulated as equivalence to the highest count value of the counter used. Fig.2 depicts the diagram of the Counter based DPWM. The working of CDPWM is that the comparator at the top evaluates the zero match of the counter to act as the SET signal. The

bottom comparator calculates the DC match of the counter and the duty cycle to serve as the RESET signal. These two signals are fed into the SR-Flip Flop.

Fig.1 - Block Diagram for the Proposed Hybrid Digital Pulse Width Modulation Generator

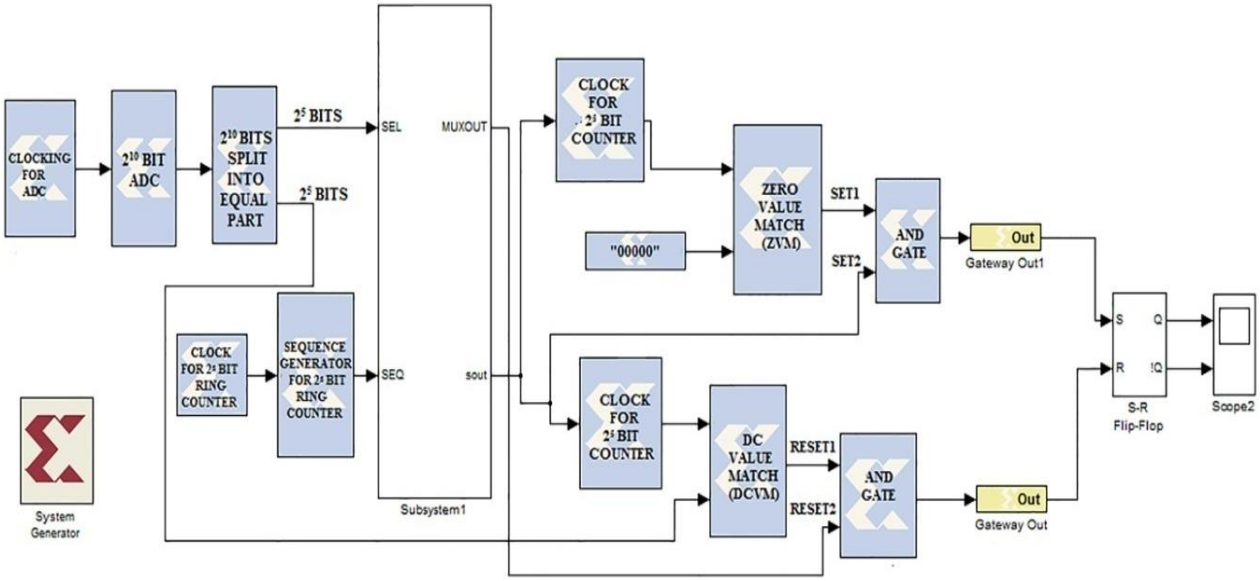
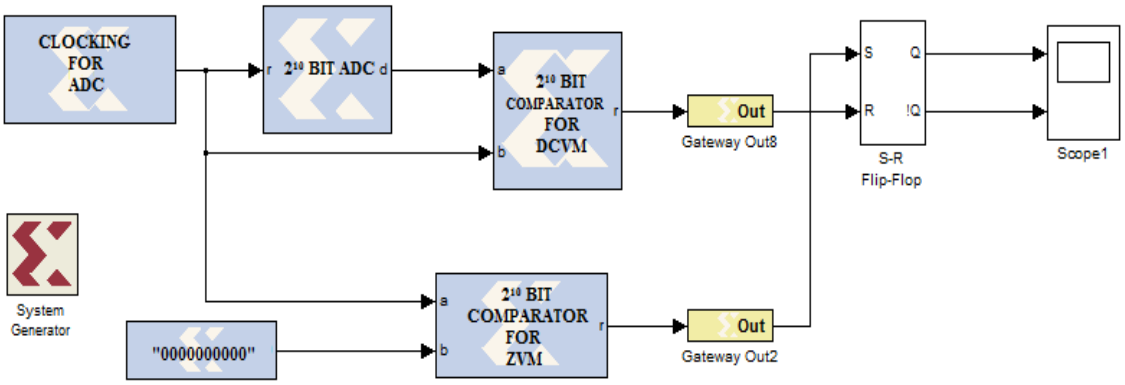



Fig. 2 - Block Diagram for Counter Based Digital PULSE Width Modulation




## c) Delay Line Digital Pulse Width Modulation Generator

Fig.3 depicts the block diagram for the 210-bit resolution Delay line-based DPWM algorithm. Digital circuits such as 210-bit ring counter, 1024:1 MUXs, and SR-flip flop are used in the design of DDPWM. The duty cycle with 210 bits is given as a Selection line for the MUXs and concurrently, the ring counter is interfaced with the inputs of the 1024:1 MUXs as shown in Fig.4. The DDPWM generates the SET signal from the 1023rd output of the ring counter through the D-Flip Flop. For the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RESET signal, the output of the 1024:1 MUXs is considered. These SET and RESET signals are fed to the SR flip flop to generate the DDPWM signal.

Fig. 3 - Block Diagram for Delay Line Based Digital Pulse Width Modulation

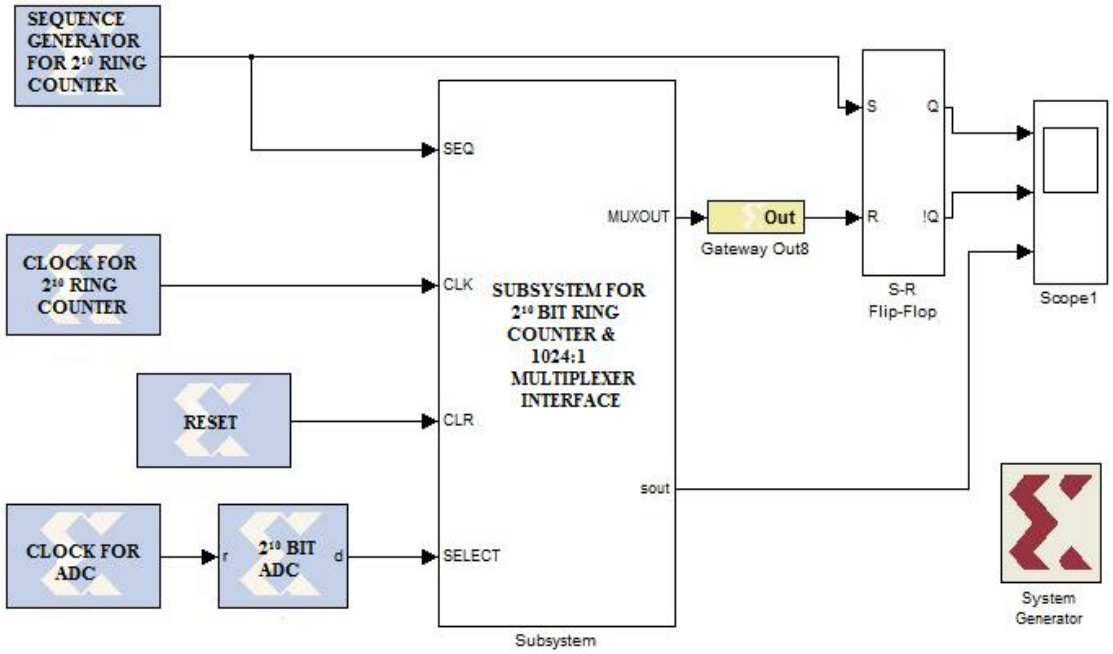
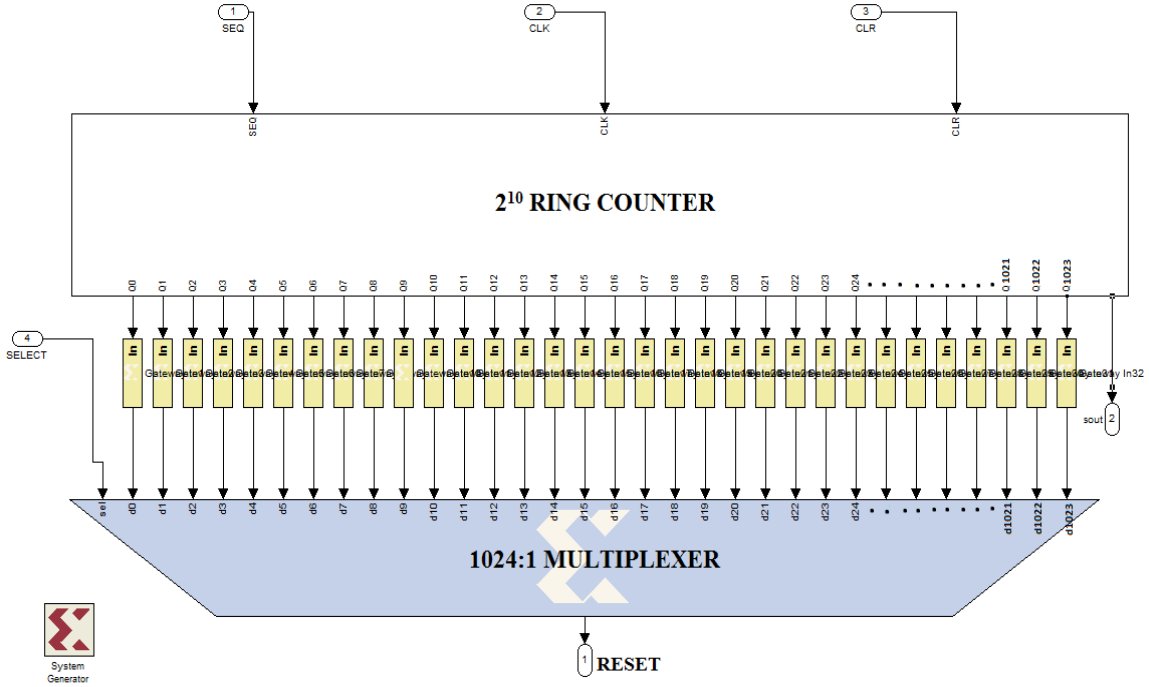



Fig. 4 - Block Diagram for $2^{10}$ Ring Counter and 1024:1 Multiplexer Subsystem





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## 3. The Proposed Triple Modular Redundancy based Hybrid Digital Pulse Width Modulation Generator

The designed HDPWM is analyzed for fault using the TMR algorithm as shown in Fig.5. The TMR considered the three times of the design under test. In this case, the HDPWM generator is the design under test and thus it is taking three times as depicted. The output of the three HDPWM is checked for fault using the Majority Voter circuit. The Majority Voter circuits are designed based on the majority correctness in the output of the HDPWMs. If suppose, a fault occurs in the topmost HDPWM (say), the outputs of the other two HDPWMs will be the same, hence the Majority Voter will consider that the majority output of the two matching HDPWM outputs are fault free. In general, the MV considers the best of the three HDPWM outputs as the fault-free output and for the sake of indicating the error in output block is constructed. The output error will indicate when the majority of the HDPWMs is erroneous.

Fig. 5 - Block Diagram for the Proposed HDPWM Using the TMR Technique

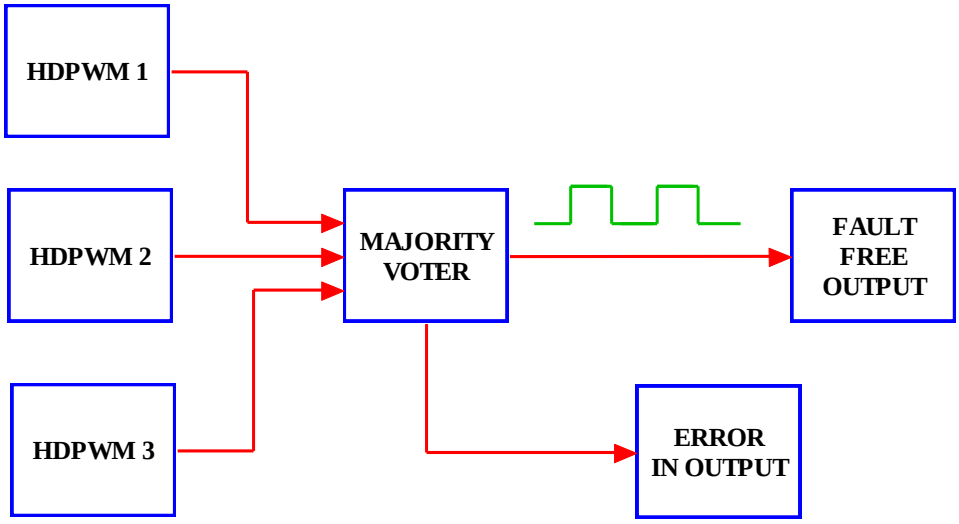


Fig.6 depicts the design flow for the proposed HDPWM based TMR for a fault-free generation. The duty cycle value is fed to the three HDPWM generators with a resolution of $2^{10}$ bits. The three HDPWMs generate the outputs at the same frequency to get the fault-free output. The operation of the HDPWM is shown in Fig.6, the $2^{10}$ values of the duty cycle are split into two parts as $2^5$ for the CDPWM and $2^5$ bits for the DDPWM. The CDPWM uses the counter and comparator circuits to produce the SET1 and RESET1. Similarly, the DDPWM utilizes the Ring Counter and Multiplexer to give the SET2 and RESET2. The HDPWM combines the pairs of SET1 & SET2 and


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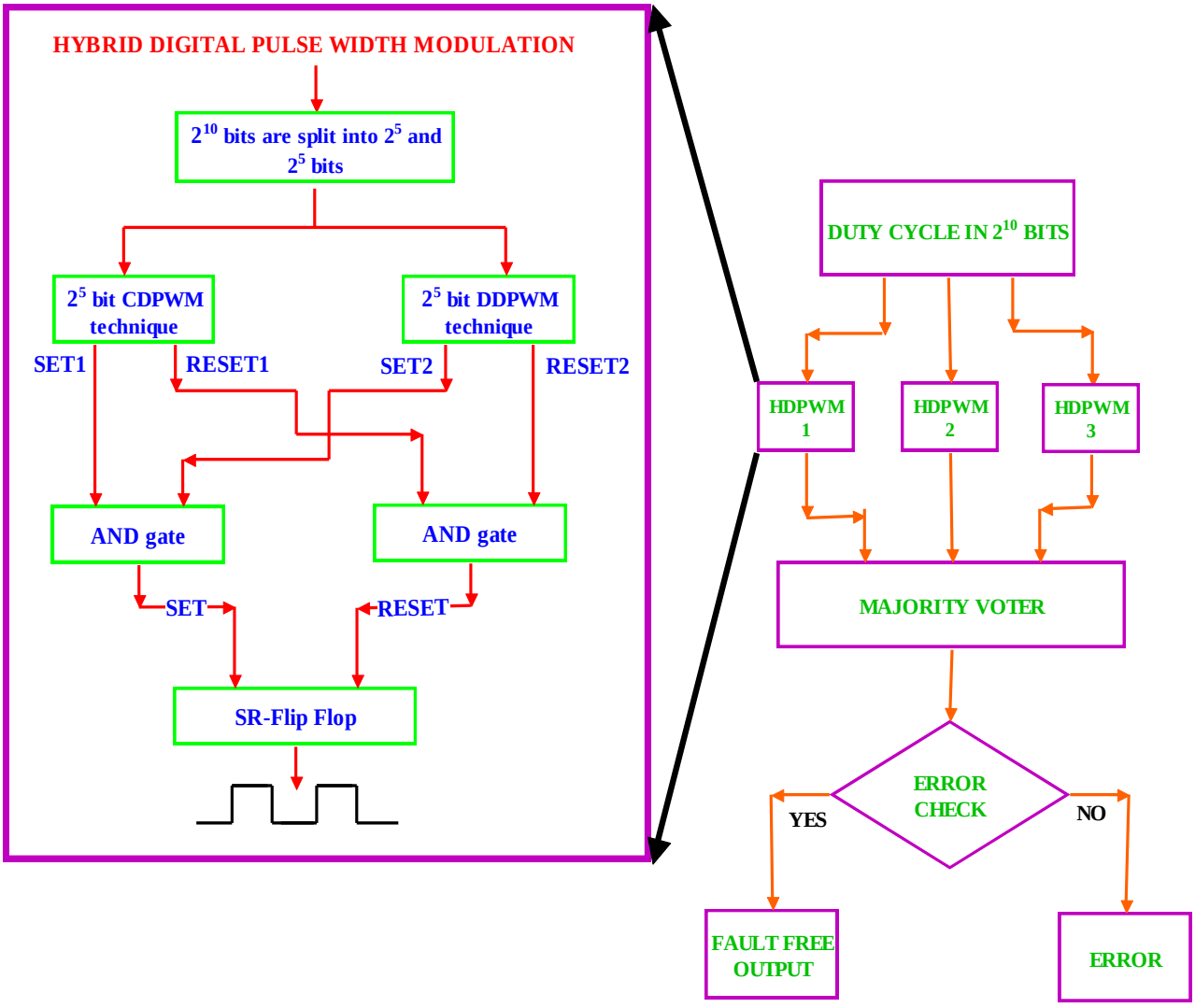
pair of RESET1 & RESET2 using the AND logic gate. The output of the two AND gates presents the SET and RESET for the SR-Flip Flop to generate the HDPWM output. The three HDPWM perform their operation to generate the three DPWM outputs to the Majority Voter Circuit. The Majority Voter checks for the fault-free output in the three HDPWM outputs and indicates the error output if any error is detected else the output is the fault-free output for the HDPWM. The Triple Modular Redundancy uses the three times of the HDPWM design that may increase the complexity for the area. But the proposed design exhibits accurate output for the HDPWM.

Fig. 6 - Flowchart for the Proposed TMR based HDPWM Generator





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## 4. Results and Discussion

The proposed HDPWM based TMR is developed using the VHDL code for the evaluation of fault-free evaluation of the output. Fig. 7 indicates the validation of the proposed method for three different conditions. The fault injection is activated to one of the duty cycle values to validate the output of the proposed method. The three conditions are assigned as given in Fig.7. The first condition is given by the duty value of 0110000100 for the HDPWM1 and HDPWM2 respectively, and the HDPWM3 with the value of 0001111001. The Majority voter produces the output corresponding to the duty values of HDPWM1 and HDPWM2. The second conditional validation is giving the duty cycle value of 0001111001 for HDPWM1 and HDPWM3 with the HDPWM2 as 1010101010. The proposed method responds to the accurate output for the duty cycles of 0001111001. The third conditional validation is considered as 1010101010 for the HDPWM2 and HDPWM3 with the HDPWM1 as 0110000100. The proposed method exhibit the majority output of the HDPWM as given in HDPWM2 and HDWPM3.

Fig. 7 - Simulation of the Proposed TMR based Hybrid Digital Pulse Modulation


The developed VHDL code for the proposed method is implemented synthesized using the Xilinx VIVADO tool. The device chosen for the evaluation is Artix 7 FPGA with the device type as xc7a100tcsg324 series. The elaborated design for the proposed method is depicted in Fig.8. The

elaborated design shows the synthesized code for the proposed method in blocks. The RTL schematic of the proposed method is also depicted in Fig. 9. The proposed method is evaluated for the power consumption using the XILINX VIVADO tool as presented in Fig. 10. The dynamic power is 1.016W and the static power is 0.095W as derived from the synthesized code of the proposed method using the XILINX VIVADO tool. The Device Utilization for the proposed method is shown in Table 1. The table depicts the minimum utilization of LUTs and FFs as 0.07% and 0.03% respectively for the proposed method.

Fig. 8 - Elaborated Schematic for the Proposed TMR based Hybrid Digital Pulse Modulation

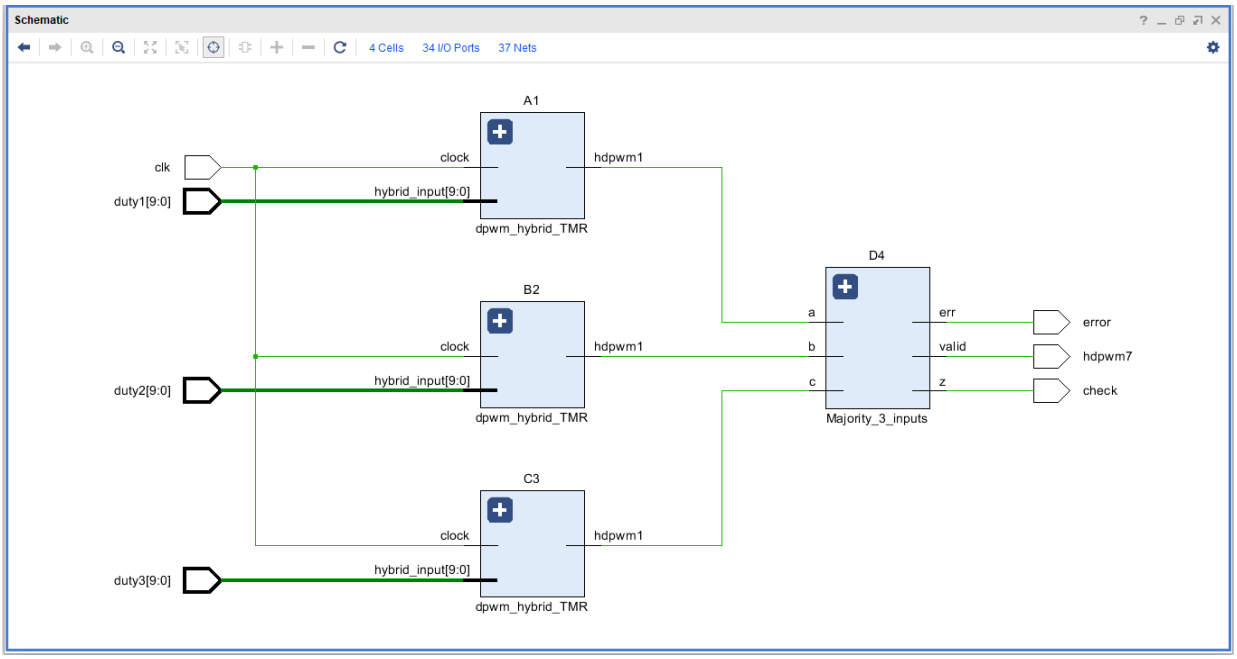


Fig. 9 - RTL Schematic for the Proposed TMR based Hybrid Digital Pulse Modulation

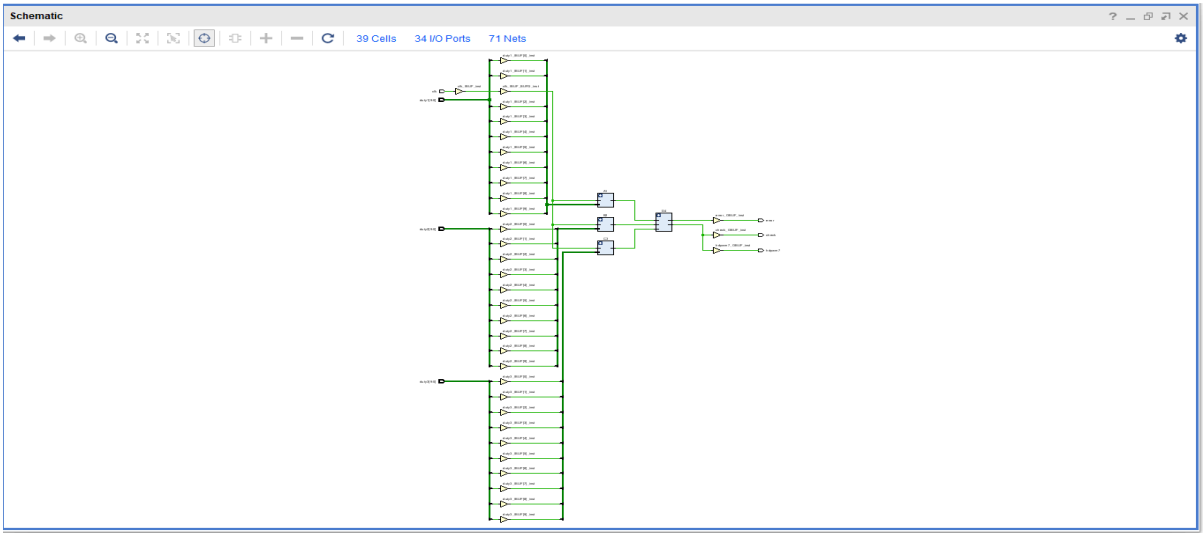



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Fig. 10 - Power Report for the Proposed TMR based Hybrid Digital Pulse Modulation

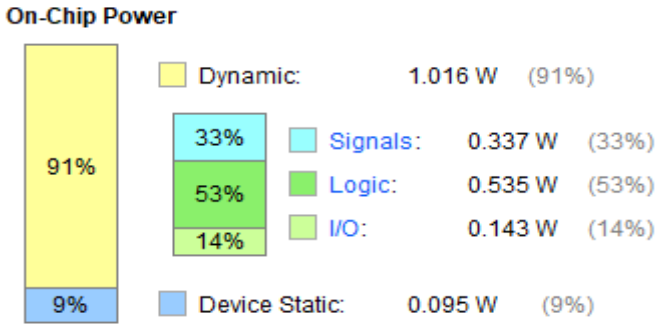


Table 1 - Device Utilization Chart for the proposed TMR based Hybrid Digital Pulse Modulation

| Resource | Utilization | Available | Utilization % |
|---|---|---|---|
| LUT | 44 | 63400 | 0.07 |
| LUTRAM | 6 | 19000 | 0.03 |
| FF | 36 | 126800 | 0.03 |
| IO | 34 | 210 | 16.19 |
| BUFG | 1 | 32 | 3.13 |

## 5. Conclusion

The proposed Triple Modular Redundancy algorithm for Hybrid Digital Pulse Width Modulation was successfully validated using the FPGA device. The synthesizable VHDL code for the proposed method is evaluated for the power and area. The dynamic power consumption of the proposed methods is as low as 1.016 W and the FF utilization is 0.03% only. The results obtained for the proposed methods are satisfactory and prove to be feasible. Future work could be directed towards the modified TMR algorithm for the validation of an advanced digital modulation generator using the FPGA device.

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