

# Simulation of Carbon Nanotube based Field Effect Transistor by Varying Gate Oxide Thickness to Explore its Electrical Property and Compare it with Standard Mosfet

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## Abstract

Aim: The current and voltage characteristics of CNTFET and MOSFET are simulated by varying their gate oxide thickness ranging from 3.5nm to 11.5nm. Materials and Methods: The electrical conductance of CNTFET (n = 320) was compared with MOSFET (n = 320) by varying gate oxide thickness ranging from 3.5nm to 11.5nm in the NanoHUB© tool simulation environment. Results: CNTFET has significantly higher conductance (12.52 mho) than MOSFET (12.07 mho). The optimal thickness for maximum conductivity was 4nm for CNTFET and 3.5 nm for MOSFET. Conclusion: Within the limits of this study, CNTFET with the gate oxide thickness of 4 nm offers the best conductivity.

**Key-words:** Carbon Nanotube Field Effect Transistor (CNTFET), Gate Oxide Thickness, Drain Current, Conductance, Nanotechnology, Novel Transistor.

# 1. Introduction

Current-voltage characteristics and conductance of CNTFET and MOSFET were analyzed by varying the gate oxide thickness (Ahmed et al. 2015). CNTFET has less power consumption and propagation delay when compared to MOSFET (Singh, Khosla, and Raj 2016). CNTFET operates at very less sub-threshold voltage hence consumes very less power during their operation than MOSFET whose threshold voltage is high (Sayed, Abutaleb, and Nossair 2016). Because of better electrical

properties, CNTFET is used in high-performance digital circuits (Karimlee and Naeini 2016). CNTFET is also used in operational amplifiers in analog circuits (Sayed, Abutaleb, and Nossair 2016; Puri and Rana 2015), (Raj, Khosla, and Singh 2019).

Many articles were published in various journals on CNTFET technology in the past 5 years. 69 research articles were published in IEEE explore and 106 research articles were published in science direct. Vishesh Dokania et. al; proposed a computationally efficient analytical model to accurately predict the electrical characteristics of wrap-gate carbon nanotube FETs (CNTFETs) (Dokania et al. 2016). Zahra Davari Shalamzari et al- designed half-adders and multiplexers and simulated in HSPICE for various load capacitors, supply voltage, process variations, frequency, and temperature ("Newly Multiplexer-Based Quaternary Half-Adder and Multiplier Using CNTFETs" 2020). Sashi Bala et al explained the design of CNTFET and explored the effect of polarity, gate bias on its performance (Bala and Khosla 2018).

Previously our team has a rich experience in working on various research projects across multiple disciplines (Sathish and Karthick 2020; Varghese, Ramesh, and Veeraiyan 2019; S. R. Samuel, Acharya, and Rao 2020; Venu, Raju, and Subramani 2019; M. S. Samuel et al. 2019; Venu, Subramani, and Raju 2019; Mehta et al. 2019; Sharma et al. 2019; Malli Sureshbabu et al. 2019; Krishnaswamy et al. 2020; Muthukrishnan et al. 2020; Gheena and Ezhilarasan 2019; Vignesh et al. 2019; Ke et al. 2019; Vijayakumar Jain et al. 2019; Jose, Ajitha, and Subbaiyan 2020). Now the growing trend in this area motivated us to pursue this project.

Although CNTFET has some good electrical properties, one of its drawbacks is off-state current leakage which can be rectified by implementing asymmetric gates in its geometry (Srimani et al. 2019). Deepak et al. have published a paper "Nanomaterial based non-destructive evaluation sensor for defect detection and strain measurements" in the journal of nanostructured polymers and nanocomposites. The main aim of this work is to simulate the current and voltage characteristics of CNTFET by varying the gate oxide thickness from 3.5nm to 11.5nm and compare with standard MOSFET for optimizing conductivity (Tiwari, Agarwal, and Saxena 2019).

# 2. Materials and Methods

All the simulations are carried out using the online simulation tool "NanoHUB©" and this work is divided into two groups. The first group refers to CNTFET and the second group refers to MOSFET. The pre-test analysis was done using clinicalc.com by keeping g-power at 80%, threshold

at 0.05%, confidence interval at 95% (Shaukat, Umer, and Islam 2017), (Salcines, Kruglov, and Kallfass 2018). Each group consists of 320 samples. So the total sample size is 640.

Simulation of CNTFET for different gate oxide thicknesses is done by opening the simulation tool in the browser. On the homepage, go-to resources and select tools from the catalog opened. CNTFETs is selected from the list of tools and then the CNTFET lab tool is launched by clicking on the launch tool button. In the tool environment, gate oxide thickness is varied from 3.5nm to 11.5 nm in the exterior settings by increasing 0.5 nm each time and simulated to get the results for each value.

For the simulation of current and voltage characteristics of MOSFET in NanoHUB© simulation tool similar steps are followed as that of CNTFET, the only change is instead of the CNTFET tool MOSFET tool is launched and simulated to get the current-voltage characteristics curve for various values of oxide thicknesses.

NanoHUB© is an in-browser simulation software tool that consists of numerous tools for nanotechnology. It is a science and engineering gateway comprising several resources that are useful for educational and research purposes (Russell and Cohn 2012). Since it is a software tool the results are precise and accurate. After the simulation current and voltage characteristics curves of CNTFET and MOSFET are obtained. The values of drain current are noted by keeping the gate voltage constant ( $V_g$ =0.65v). The conductance of both CNTFET and MOSFET is obtained by calculating the ratio between drain current and gate voltage (Rouf et al. 2014). For statistical analysis origin pro V80 and SPSS software are used in this work. The conductance of both CNTFET and MOSFET for different oxide thicknesses was plotted using origin software. Compare drain current and conductance of CNTFET and MOSFET by using Independent T-test in the SPSS software data analysis tool. Gate voltage and gate oxide thickness are considered as independent variables and drain current and conductance as dependent variables.

### 3. Results

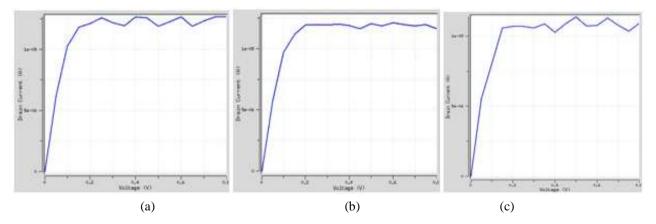
The values of drain current are measured from current-voltage characteristics curves of CNTFET (Fig 1). Conductance values are obtained from the simulation by keeping gate voltage as 0.65V and the respective values are tabulated (Table 1). From the graphical representation of conductivity of CNTFET (Fig 2), it can be observed that the conductance and drain current of CNTFET slightly decreases as the gate oxide thickness increases. The conductance of CNTFET

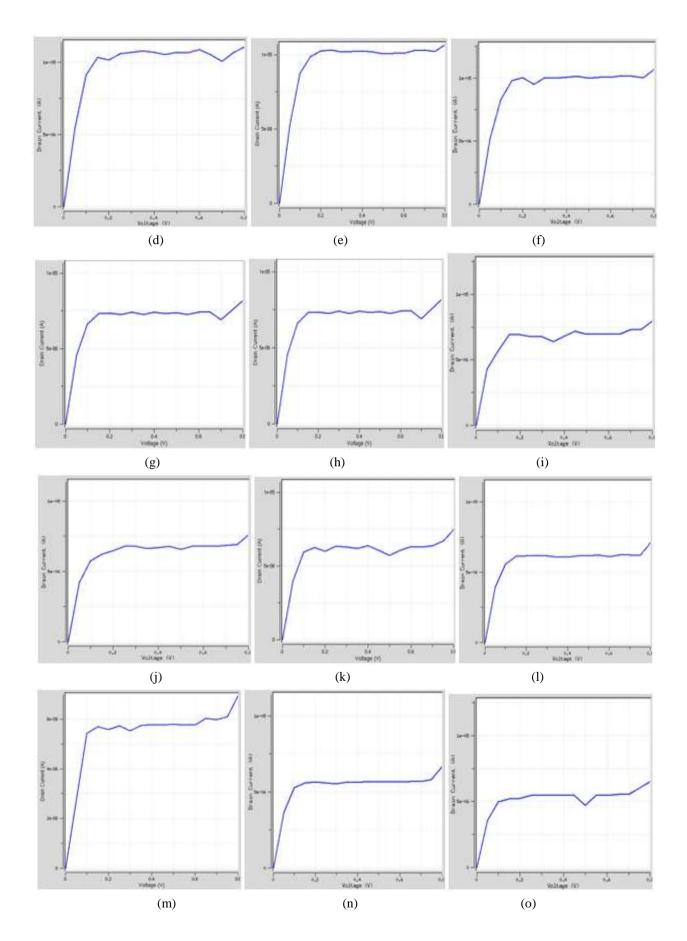
appears to be maximum (18.4554 x  $10^{-06}$  mho) when gate oxide thickness is 4 nm and appears to be the minimum value of 7.9477 x  $10^{-06}$  mho for gate oxide thickness 11.5 nm (Table 1).

Gate oxide thickness(nm)	Current (x10 <sup>-06</sup> A)	Voltage (V)	Conductance ( $x10^{-06}$ mho)			
3.5	11.9088	0.65	18.3212			
4	11.996	0.65	18.4554			
5	11.2878	0.65	17.3658			
5.5	10.5285	0.65	16.1977			
6	10.2974	0.65	15.8422			
6.5	10.1759	0.65	15.6552			
7	7.9412	0.65	12.2172			
7.5	7.4613	0.65	11.4789			
8	6.9453	0.65	10.6851			
8.5	6.787	0.65	10.4415			
9	6.3007	0.65	9.6934			
9.5	6.1999	0.65	9.5383			
10	6.0433	0.65	9.2974			
10.5	5.6761	0.65	8.7325			
11	5.5516	0.65	8.5409			
11.5	5.166	0.65	7.9477			

Table 1- Drain Current and Conductance Values for CNTFET

Fig. 1- Simulated Current-voltage Characteristics Curves of CNTFET for Gate Oxide Thickness of (a) 3.5 nm (b) 4 nm (c) 5 nm (d) 5.5 nm (e) 6 nm (f) 6.5 nm (g) 7 nm (h) 7.5 nm (i) 8 nm (j) 8.5 nm (k) 9 nm (l) 9.5 nm (m) 10 nm (n) 10.5 nm (o) 11 nm (p) 11.5 nm. Variation of Drain Current with Respect to the Gate Voltage 0 V to 1V is Plotted and Analysed





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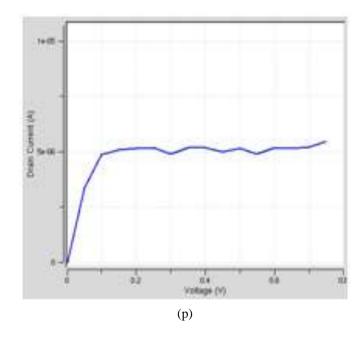


Table 2- Drain Current and Conductance Values for MOSFET

Gate oxide thickness(nm)	Current $(x10^{-06}A)$	Voltage (V)	Conductance(x10 <sup>-06</sup> mho)		
3.5	50.8846	0.65	78.284		
4	35.8221	0.65	55.1109		
5	18.2268	0.65	28.0412		
5.5	10.9583	0.65	16.8589		
6	5.6995	0.65	8.7684		
6.5	2.4998	0.65	3.8458		
7	0.945	0.65	1.4538		
7.5	0.328	0.65	0.5046		
8	0.1112	0.65	0.1711		
8.5	0.0383	0.65	0.0589		
9	0.0136	0.65	0.0209		
9.5	0.00504	0.65	0.0077		
10	0.00194	0.65	0.003		
10.5	0.00078	0.65	0.0012		
11	0.00033	0.65	0.0005		
11.5	0.00014	0.65	0.0002		

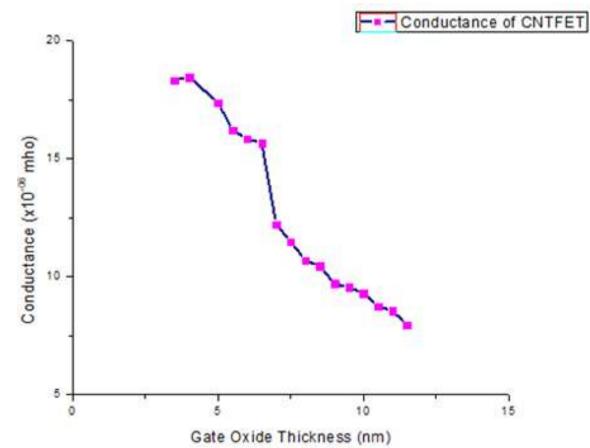
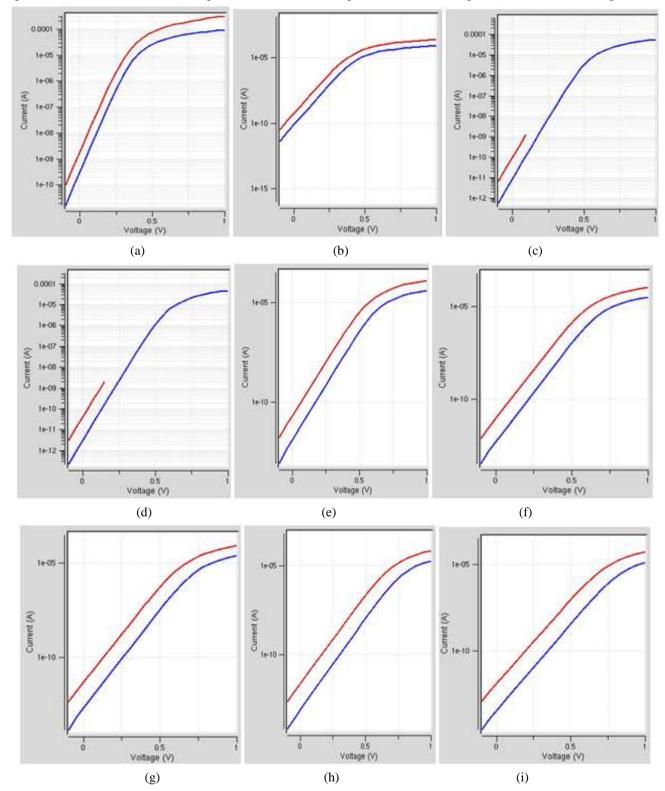


Fig. 2- Graphical Representation of Conductivity of CNTFET for Various Gate Oxide Thicknesses. Conductance is Inversely Proportional to Gate Oxide Thickness

The values of drain current are measured from current-voltage characteristics curves of MOSFET (Fig 3) by keeping gate voltage as 0.65V and the respective conductance values are tabulated (Table 2). The conductance of MOSFET is appeared to be high i.e.  $78.284 \times 10^{-06}$  mho for gate oxide thickness of 3.5nm and it appears to decreases drastically to a very less value i.e.  $0.0002 \times 10^{-06}$  mho as gate oxide thickness increases (Table 2). As per the graphical representation of conductivity of MOSFET the conductance of MOSFET appears to decrease abruptly as the gate oxide thickness increases (Fig 4). The Conductance of CNTFET appears to have the highest mean of  $12.525650 \times 10^{-06}$  mho and conductance of single gate MOSFET appears to have the lowest mean of 12.070694 mho (Table 3). The drain current of CNTFET has a mean of  $8.141675 \times 10^{-06}$  mho. The value of p is less than 0.05 (p<0.05), there is a statistically significant difference between the conductance and drain current of CNTFET (Table 4).

Fig. 3- Simulated Current and Voltage Characteristics of MOSFET for Oxide Thickness of (a) 3.5nm (b) 4nm (c) 5nm (d) 5.5nm (e) 6nm (f) 6.5nm (g) 7nm (h) 7.5nm (i) 8nm (j) 8.5nm (k) 9nm (l) 9.5nm (m) 10nm (n) 10.5nm (o) 11nm (p) 11.5nm. **Red** line Represents IV Curve with Drain Voltage of 1v and **Blue** Line Represents Current-voltage Curve with Drain Voltage of 0.05v



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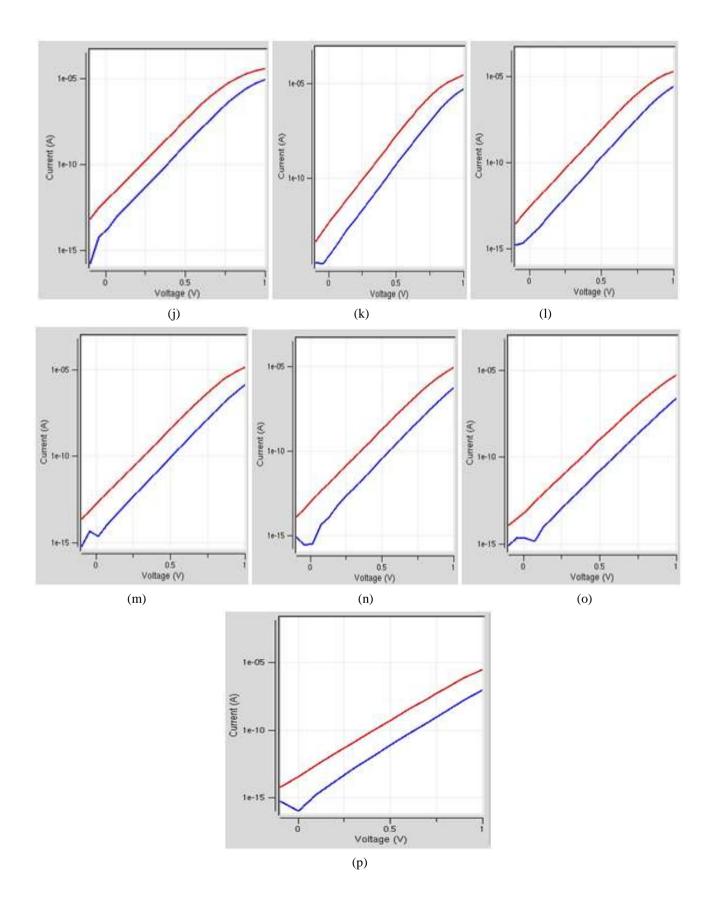


Fig. 4- Graphical Representation of Conductivity of MOSFET for various Gate Oxide Thicknesses. The Conductance of MOSFET is Inversely Proportional to Gate Oxide Thickness

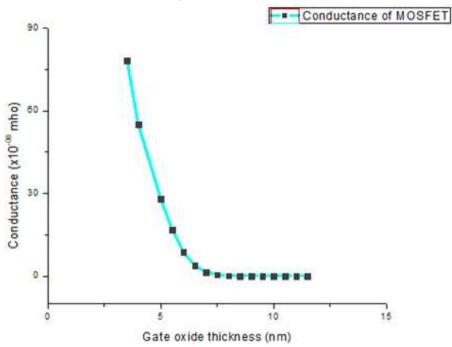


Fig. 5- Comparison of Conductance of CNTFET and MOSFET. The Conductance of Both CNTFET and MOSFET Decreases with an Increase in Gate Oxide Thickness. The **Red** Line Represents MOSFET and the **Blue** Line Represents CNTFET

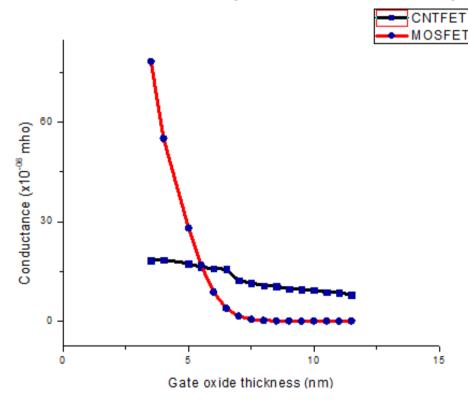


Fig. 6- Bar Chart Comparing the Mean (+-1SD) Conductance and Drain Current of CNTFET and MOSFET by Varying Oxide Thickness. There is a Significant difference between the Two Groups p<0.05 (Independent Sample T-Test). X-AXIS: CNTFET vs MOSFET. Y-AXIS: Mean of Drain Current and Conductance

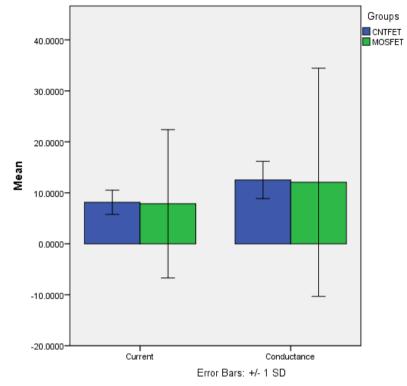


Table 3- T-Test Comparison of Conductance of CNTFET and MOSFET by Varying Gate Oxide Thickness from 3.5nm to 11.5nm. There is a Statistically Significant difference in Conductance of CNTFET and MOSFET. The Conductance of CNTFET has the Highest Mean 12.525650 x10<sup>-06</sup> mho and MOSFET has the Lowest Mean 12.070694 x10<sup>-06</sup> mho. The Drain Current of CNTFET has a Mean of 8.141675 x10<sup>-06</sup> mho which is Higher and MOSFET has the Lowest Mean of 7.845964 x10<sup>-06</sup> mho

	Group	Ν	Mean	Std. Deviation	Std. Error Mean
Current	CNTFET	320	8.141675	2.3807208	.1330863
	MOSFET	320	7.845964	14.5562737	.8137204
Conductance	CNTFET	320	12.525650	3.6626421	.2047479
	MOSFET	320	12.070694	22.3942691	1.2518777

Table 4- Mean, Standard Deviation, and Significant difference of Conductivity and Drain Current for CNTFET and MOSFET.There is a Significant difference between the Two Groups Since p<0.05 (Independent Sample T-Test)</td>

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		Levene's Test for Equality of Variances		T-test for Equality of means						
		F	Sig	t	dif	Sig (2- tailed)	Mean Difference	Std Error Difference	95% Confidence Interval of the Difference Lower Upper	
Current	Equal variances assumed Equal variances not assumed	223.534	.000	0.359 0.359	638 336.054	0.728 0.720	0.2957106 0.2957106	0.8245319 0.8245319	- 1.3234139 - 1.3261835	1.9148151 1.9176047
Conductan ce	Equal Variances assumed Equal Variances not assumed	223.534	.000	0.359 0.359	638 336.054	0.720 0.720	0.4549562 0.4549562	1.2685107 1.2685107	- 2.0360046 - 2.0402656	2.9459171 2.9501781

### 4. Discussion

Current and voltage characteristics of CNTFET and MOSFET were analyzed by varying the gate oxide thickness of the device (Sanjeet Kumar Sinha and Chaudhury 2014). Drain current vs gate voltage characteristics have been simulated for different gate oxide thickness of the device ranging from 3.5 nm to 11.5 nm. As the gate oxide thickness increases the conductivity and the drain current of CNTFET and MOSFET decreases (Das and Kundu 2012). After analyzing the current-voltage characteristics curves, it has been observed that lowering the oxide thickness of the gate will increase drain current which ultimately increases the conductivity for both CNTFET and MOSFET (Sanieet Kumar Sinha and Chaudhury 2014), (Venkataiah 2019). Even though the conductance value of MOSFET for gate oxide thickness 3.5 nm appears to be high, practically for low values of gate oxide thickness in MOSFET results in gate current leakage due to tunneling effect (Sanieet Kumar Sinha and Chaudhury 2014), (Barletta and Ngwan 2016) also presented the same in their works. So to avoid tunneling effect in MOSFET gate oxide thickness should be high but for higher oxide thickness current and conductance values are very less. In the case of CNTFET, there is only a slight decrease in current and conductance when the oxide thickness is increased.

Factors affecting the conductivity and drain current of CNTFET and MOSFET are source/drain length, channel length, device-width, and gate voltage. Modifying any of these factors can result in a change of drain current and conductance of both the transistors. So precautions were taken to keep all these constant for both CNTFET and MOSFET during the sample preparation. So source/drain length, channel length, device-width, and gate voltage will have the same effect on all the samples and hence the outcome will not get affected.

Our institution is passionate about high quality evidence based research and has excelled in various fields (Vijayashree Priyadharsini 2019; Ezhilarasan, Apoorva, and Ashok Vardhan 2019; Ramesh et al. 2018; Mathew et al. 2020; Sridharan et al. 2019; Pc, Marimuthu, and Devadoss 2018; Ramadurai et al. 2019). We hope this study adds to this rich legacy.

Limitations such as short channel effect, less range of oxide thickness, subthreshold conduction should be taken into consideration. It is evident from the findings that the overall conductance of the CNTFET is higher than that of the MOSFET. It is also seen that MOSFETs seem to have a more standard deviation in both drain current and conductance values. But CNTFET appears to have very less deviation in drain current and conductance. Hence, novel transistors like CNTFET have stable, better conductance than MOSFET.

CNTFET is one of the most promising emerging innovations that could eventually replace silicon-based electronics in the future.

#### 5. Conclusion

CNTFET gives better conductivity and performance when provided with the same gate voltage. The variation in current and voltage characteristics of CNTFET and MOSFET were analyzed and results of CNTFET were compared with MOSFET by keeping gate voltage as constant (0.65v). The conductance of both CNTFET and MOSFET decreases as oxide thickness increases. To improve the conductivity of CNTFET and MOSFET the oxide thickness should be minimum. Even though conductance can be increased by decreasing oxide thickness of both field-effect transistors CNTFET is preferred over MOSFET due to current leakage in MOSFET.

#### **Declarations**

#### **Conflict of Interests**

No conflict of interest in this manuscript.

### **Author Contribution**

Author Morupuri Satish Kumar Reddy was involved in data collection, data analysis, manuscript writing. Author Dr. A. Deepak was involved in conceptualization, guidance and critical review of manuscript.

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All the simulations used in this research paper were carried out in NanoHUB© and the data was processed in the tool and graphs were generated. We would like to take this opportunity to express our gratitude to Saveetha School of Engineering's administration for providing the requisite support and motivation to complete this project.

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