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Design of High-Speed Low Power Computational Blocks for DSP Processors

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Abstract

In today's deep submicron VLSI (Very Large-Scale Integration) Integrated Circuits, power optimization and speed play a very important role. This importance for low power has initiated the designs where power dissipation is equally important as performance and area. Power reduction and power management are the key challenges in the design of circuits down to 100nm. For power optimization, there are several techniques and extension designs are applied in the literature. In real time Digital Signal Processing applications, multiplication and accumulation are significant operations. The primary performance criteria for these signal processing operations are speed and power consumption. To lower the power consumption, there are techniques like Multi threshold (Multi-Vth), Dula-Vth etc. Among those, a technique known as GDI (Gate diffusion Input) is used which allows reduction in power, delay and area of digital circuits, while maintaining low complexity of logic design. In this paper, various signal processing blocks like parallel-prefix adder, Braun multiplier and a Barrel shifter are designed using GDI (Gate diffusion Input) technique and compared with conventional CMOS (Complementary Metal Oxide Semiconductor) based designs in terms of delay and speed. The designs are simulated using Cadence Virtuoso 45nm technology. The Simulation results shows that GDI based designs consume less power and delay also reduced compared to CMOS based designs.

Key-words: VLSI, CMOS, Gate Diffusion Input (GDI), Braun Multiplier, Parallel-Prefix Adder.

1. Introduction

In most of the VLSI applications, like video and image processing, digital signal processing and microprocessors, various arithmetic computational blocks used are adders and multipliers.

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Digital signal processors (DSPs) are considered to be the fastest of all processors due to its ability to carry out needed mathematical operations.

For a given application, one can choose the type of DSP based on such factors as speed, throughput, arithmetic capability, precision, size, cost and power consumption. As the technology grows, there are more and more such devices with better and better performance characteristics that are easily incorporated in DSP systems. As the technology is growing, the speed requirements are increasing heavily. To reach such high-performance desires, many alternate techniques have been adopted by current researchers. Many industries are trying to improve their technology and devices considering greater complexity. It means more functionality, higher density in order to place millions of transistors on a lesser die area, increased performance and lower power dissipation [1].

While improving speed of device, power issues also arise. However, both speed and power have to be optimized in order to achieve desired performance gains [2]. Some of the techniques to reduce the power are transistor stacking, Multi-Threshold (Multi-Vt), True single-phase clock (TSPC) logic and so on. Gate Diffusion Input (GDI) is one among the practically implementable technique to reduce power consumption in switching circuits. This GDI method makes use of a simple cell to design low-power logic gates that results in chip area reduction and less complexity.

In the literature, several researchers designed various digital circuits and computational blocks based on GDI technique independently and compared with that of conventional CMOS technique. In this paper, various computational blocks suitable to DSP processors such as Kogge-Stone Adder, Braun Multiplier and Mux based barrel shifter by making use GDI technique are designed and simulated which guaranteed in low power and high speed.

This paper is as organized as follows. Basic Computational Blocks for DSP processors are briefed in section II. The salient features of GDI Technique are discussed in Section III. Section IV concentrates on results and discussion. This paper is concluded in Section V.

2. Basic Computational Blocks

The hardware building blocks that are essential to carry out basic DSP computations are Adders, Multipliers and Shifters. Designing these blocks at device level is always a challenging task. While choosing these hardware computational building blocks, the key issues to be considered are power, speed and area.

Adder

In most of the DSP applications such as Multipliers and MAC units, adders are mandatory blocks. There are many styles of adders till now. However, the technology requires more optimized adder in order to reach its level of desires. To do so, parallel prefix adders are introduced. Parallel prefix adders are those adders which overcomes the standard problems as speed and power consumption of conventional adders.

The parallel prefix adder employs the 3-stage structure of the CLA adder. Key architectures of Parallel- prefix adder incudes Kogge Stone adder, Ladner-Fisher adder, Brent-Kung adder. Among them, Kogge Stone Adder is one that operates with high processing speed. The main advantage of this adder is it avoids the delay due to propagation of carry.

Multiplier

The main reasons for the availability of commercial VLSI chips capable of realizing DSP functions are the arrival of single chip multipliers and their integration into processor architecture. Such multipliers can be called as parallel prefix multipliers. These multipliers complete multiplication operation to generate product of two binary numbers in a single processor cycle.

An array multiplier is a combinational circuit used to multiply two binary numbers digitally by employing an array of half adders and full adders. The most popular Array multipliers are Wallace Tree multiplier, Braun Multiplier, Baugh Wooley multiplier. Among them Braun Multiplier is one of the most popular Array Multiplier widely used in DSP processors such as TMS320C54XX. It has the basic architecture derived from manual operation of 2 bit multiplication. It includes array of array of AND gates and Full adders.

Barrel Shifter

In earlier processors, shifting operation is conventionally implemented using a shift register. Since it takes single clock to shift single bit, average shifting delay is more. This must be reduced.

Barrel Shifter improves shifting efficiency in high speed DSP processors.

Barrel shifter circuit implementation is one way of reducing its delay. It shifts several bits in single clock. Number of shifts can be determined by control inputs [3].

3. GDI Technique

Gate Diffusion Input (GDI) is a well-known technique in low power digital IC design. The overall power consumption of the circuit can be reduced by using this technique. Meanwhile it significantly contributes improvement in delay and area of the circuit [4]. Figure 1 shows a simple GDI cell.

A GDI cell can be simply described as CMOS inverter without separate DC power supply. This primitive cell has three inputs and an output. These three inputs can be configured to get the logic of basic gates as mentioned in table 1.

Fig.1 -Simple GDI Cell

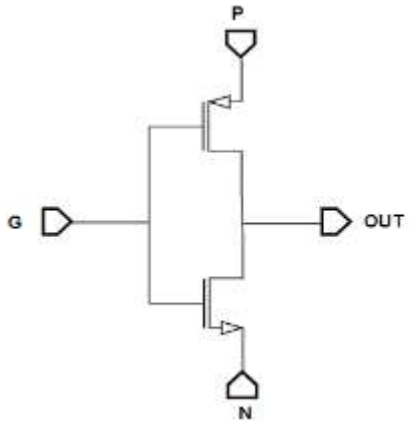

Table I- Different Logic Functions for Various Input Combinations

N	P	G	OUT
0	B	A	A'B
B	1	A	A'+B
1	B	A	A+B
B	0	A	AB
0	1	A	A'

Since the basic GDI contains no VCC separately, there is a loss in voltage swing. To avoid this new modified are proposed in literature. To take care of this voltage loss, a new transistor can be connected at output side. This in turn increases transistor count to 3 from 2 for basic gates. Moreover the gate operation purely depends upon the Fabrication parameters such as W/L ratio.

4. Results and Discussions

All design blocks are simulated in cadence virtuoso 45nm technology. For every schematic, transient response with overall delay, power and transistor count are reported as follows.

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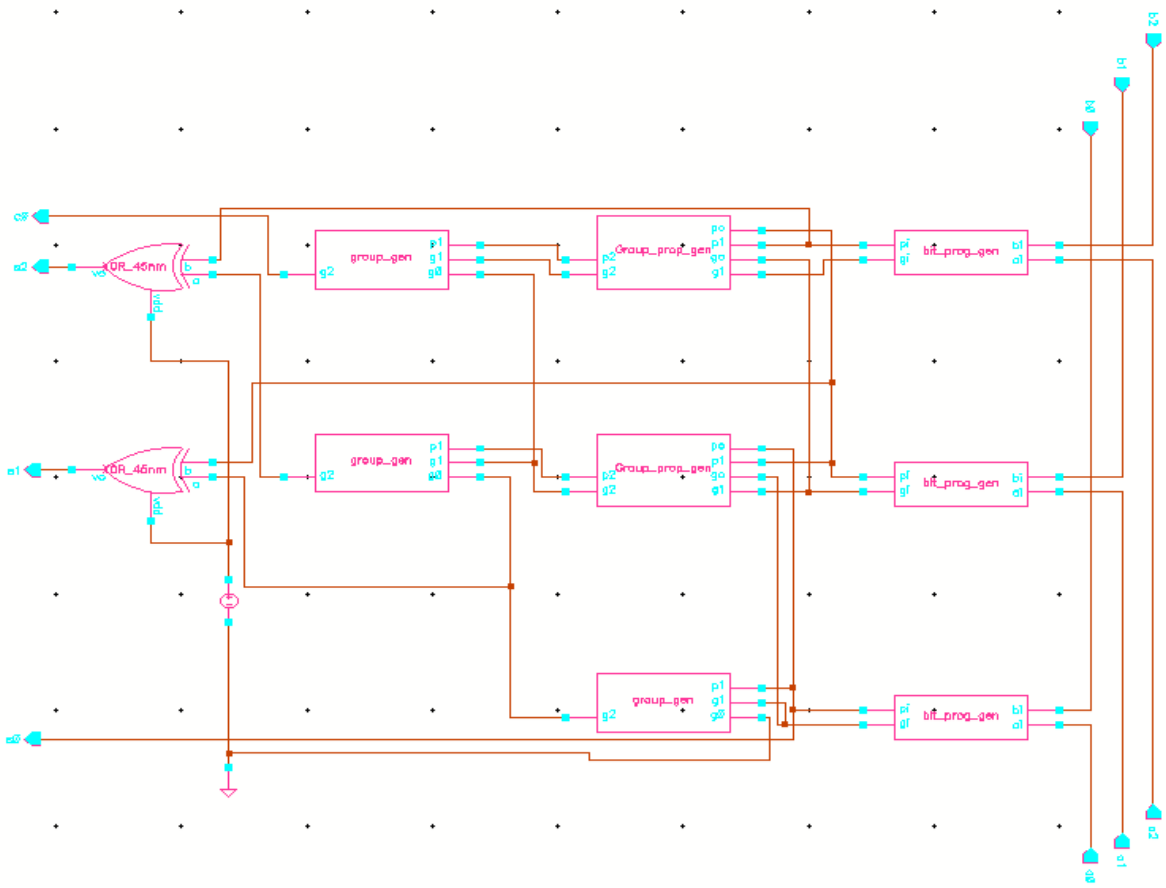
Kogge-Stone Adder

It is considered as one of the quickest parallel prefix adder, which is used in most of the DSP applications. It includes following three blocks [5].

a) Bit-generation.
b) Carry-generation.
c) Carry propagation.

Here, Carry generation and propagation are same as in Carry look ahead adder. It is low depth depth adder with minimal fan-out at each node. The figure 2 shows the schematic of 3-bit KSA with two 3-input buses and one output bus with three sum bits and one carry bit. This circuit is simulated with conventional blocks and then with GDI based basic gates.

Fig. 2- Schematic of Kogge-Stone Adder



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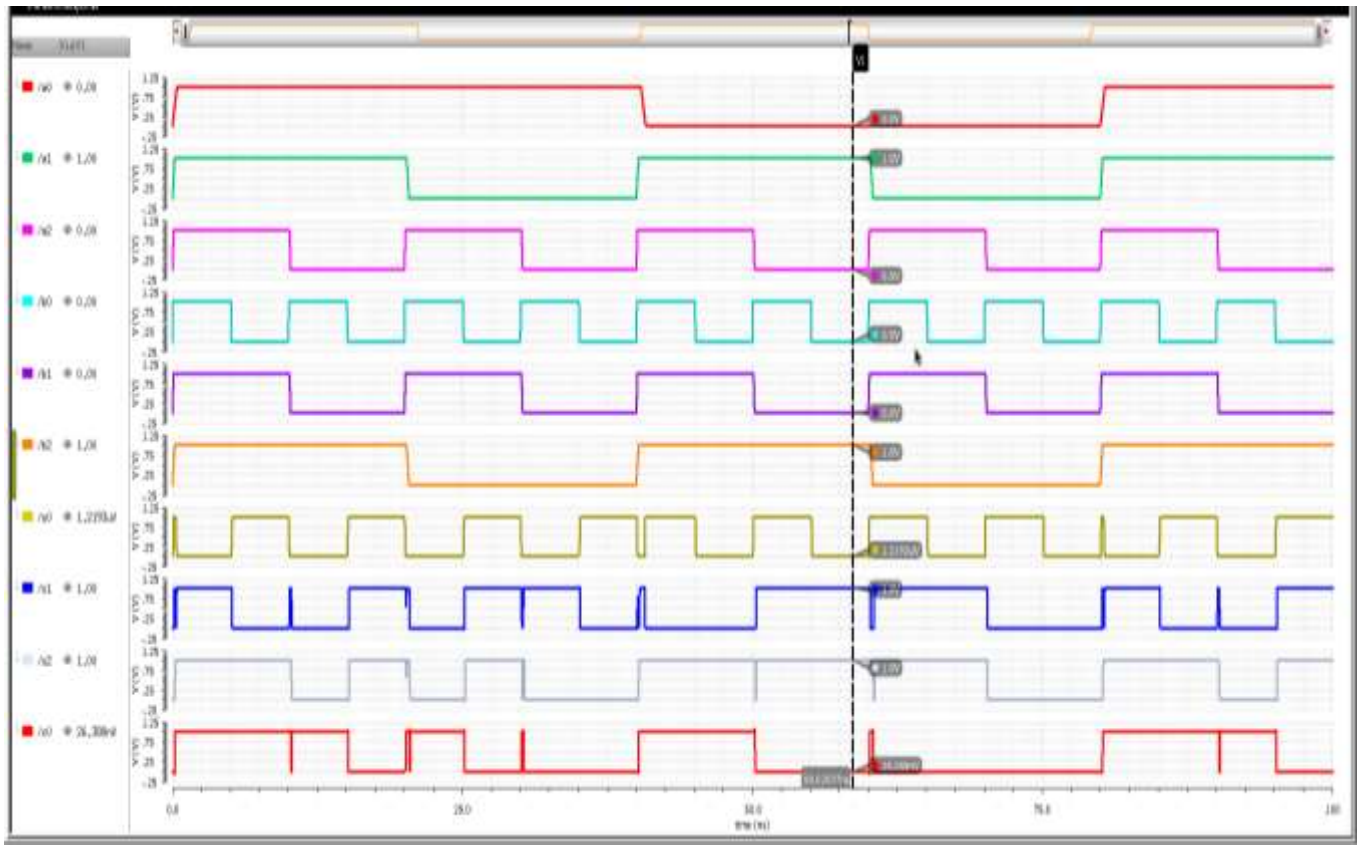
The three pre-processor blocks are designed before with basic gates then used as cells in the final schematic. Actually, all these pre-processor blocks consist of XOR gates which has more number of transistors compared to other basic logic gates. This can be reduced by designing an XOR gate using GDI technique.

Fig. 3- Transient Response of GDI based KSA



The output waveforms of GDI based KSA are shown in Figure 3. The three inputs are given with an Amplitude 1 V and time-period in the orders of pico-seconds (ps). Some of the output bits are generating spikes because of dynamic switching activity.

Braun Multiplier with KSA

A 4-bit Braun Multiplier is a parallel multiplier with array of Full adders and AND gates. The final stage of Braun Multiplier is the ripple carry adder, from which output bits are generated is the main reason for delay in propagation of carry. This is avoided by using a high-speed adder instead of conventional adder [6]. Since Parallel prefix adders is considered to be fastest adder, Kogge Stone Adder is used instead of conventional Ripple carry adder.

Figure 4 shows the schematic of a 4-bit Braun Multiplier in which last stage is replaced with KSA. All the blocks are designed with conventional blocks and using GDI technique.

Fig. 4- Schematic of Braun Multiplier with KSA

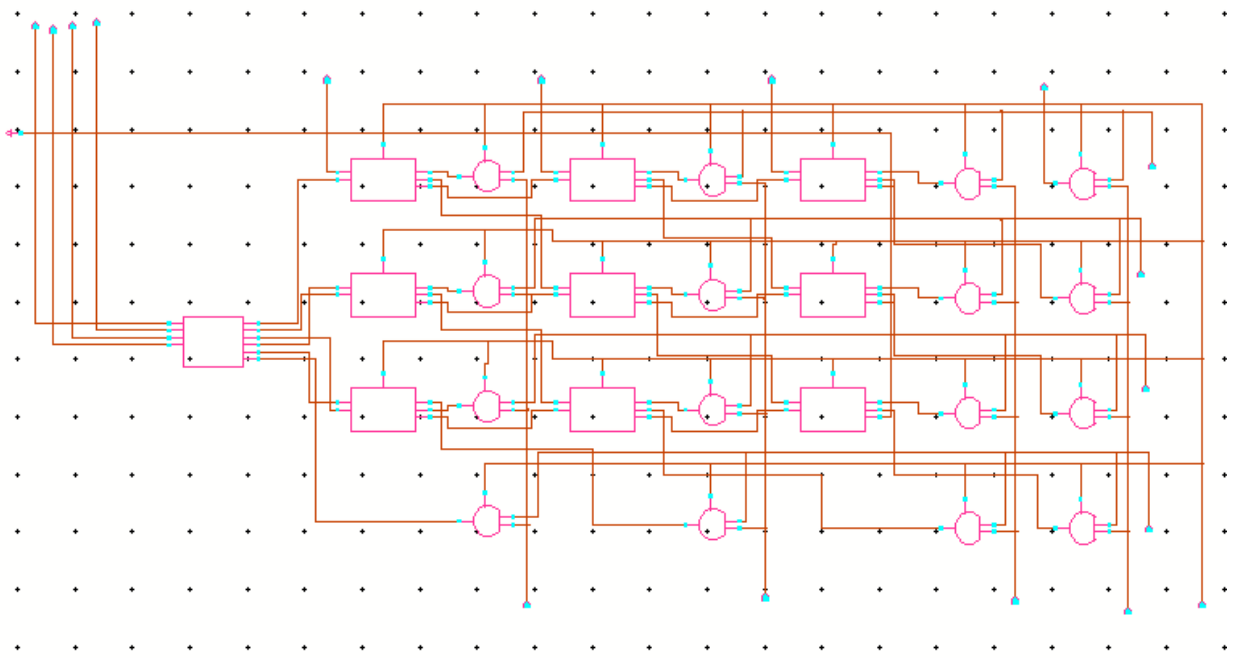


Fig. 5- Transient Response of GDI based Braun Multiplier with KSA

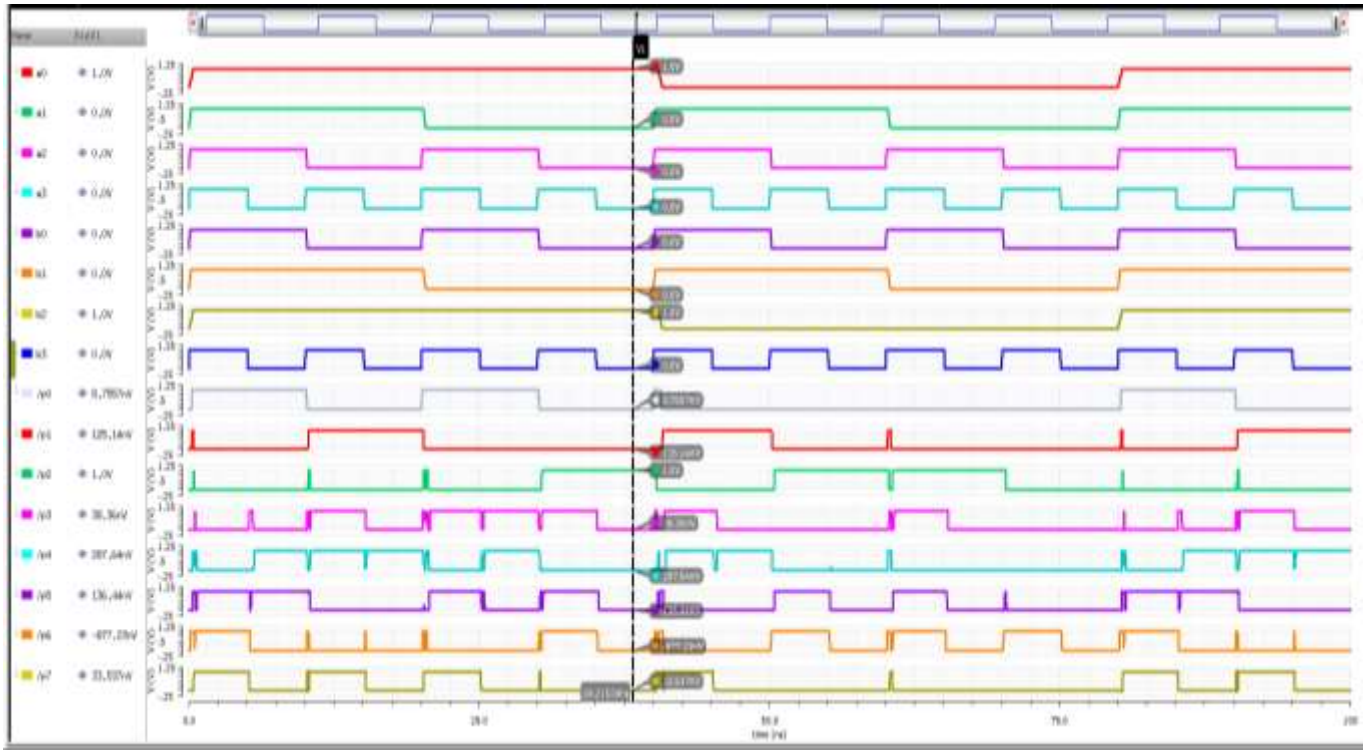


Figure 5 shows the output waveforms of GDI based Braun Multiplier with KSA. Two 4-bit inputs are given with an Amplitude 1V and time-period in the orders of pico-seconds (ps).

Barrel Shifter

A 4-bit Barrel shifter usually perform to shift inputs based on number of shifts specified. Based on control signals, Number of shifts can vary from 0 to 2n.

There are many methodologies to implement a Barrel shifter. Some of them are PTL based, Transmission gates and so on. Multiplexer based Shifters [7] leads to high-speed circuits with less number of transistors. Using low power techniques, the power can be further decreased.

MUX based Barrel shifters can be designed for low power applications with GDI logic incorporating into it. Figure 6 shows the schematic of 4-bit MUX based Barrel shifter in which multiplexers are designed with GDI technique.

Fig. 6- Schematic of Barrel Shifter with GDI Logic, based on 4-bit MUX

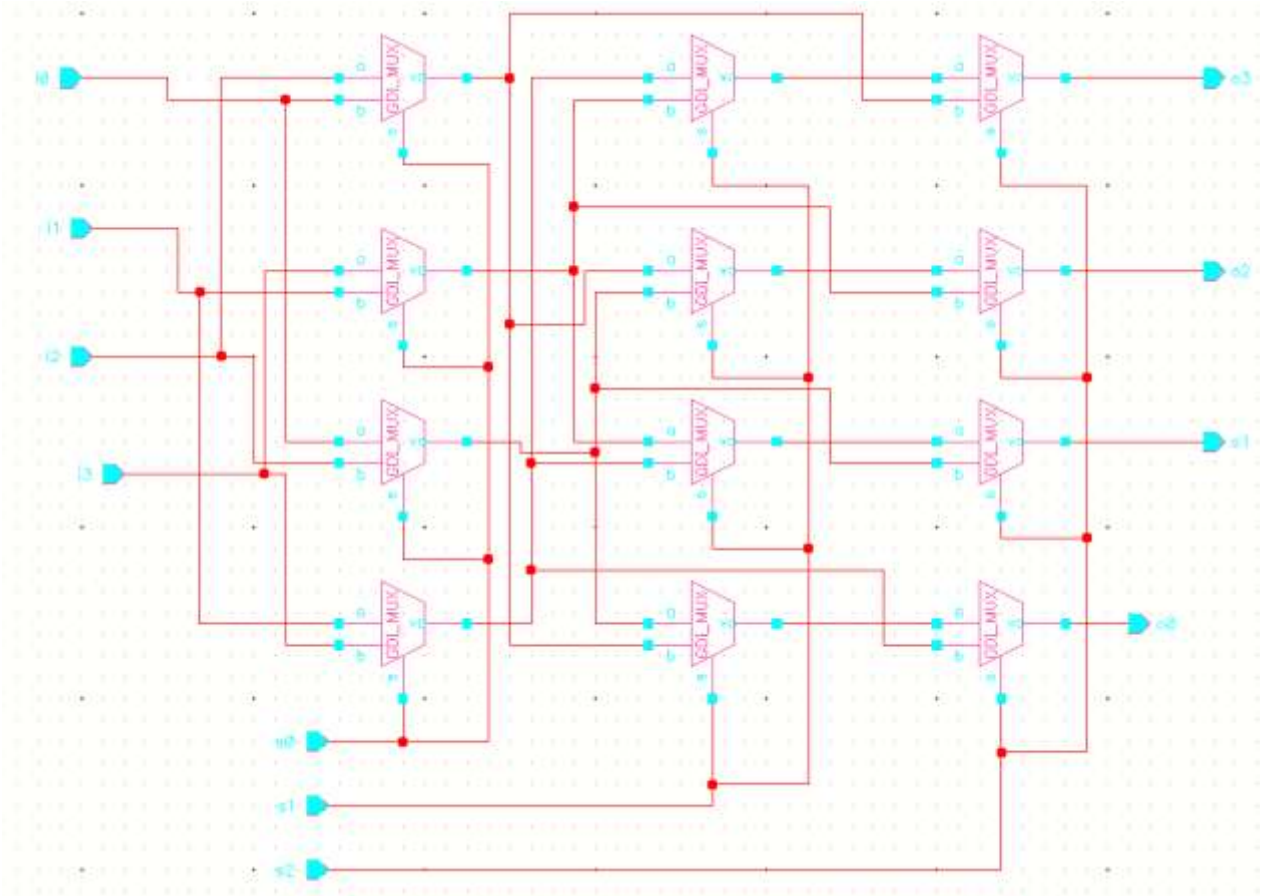


Fig. 7- Transient Response of GDI based Barrel Shifter

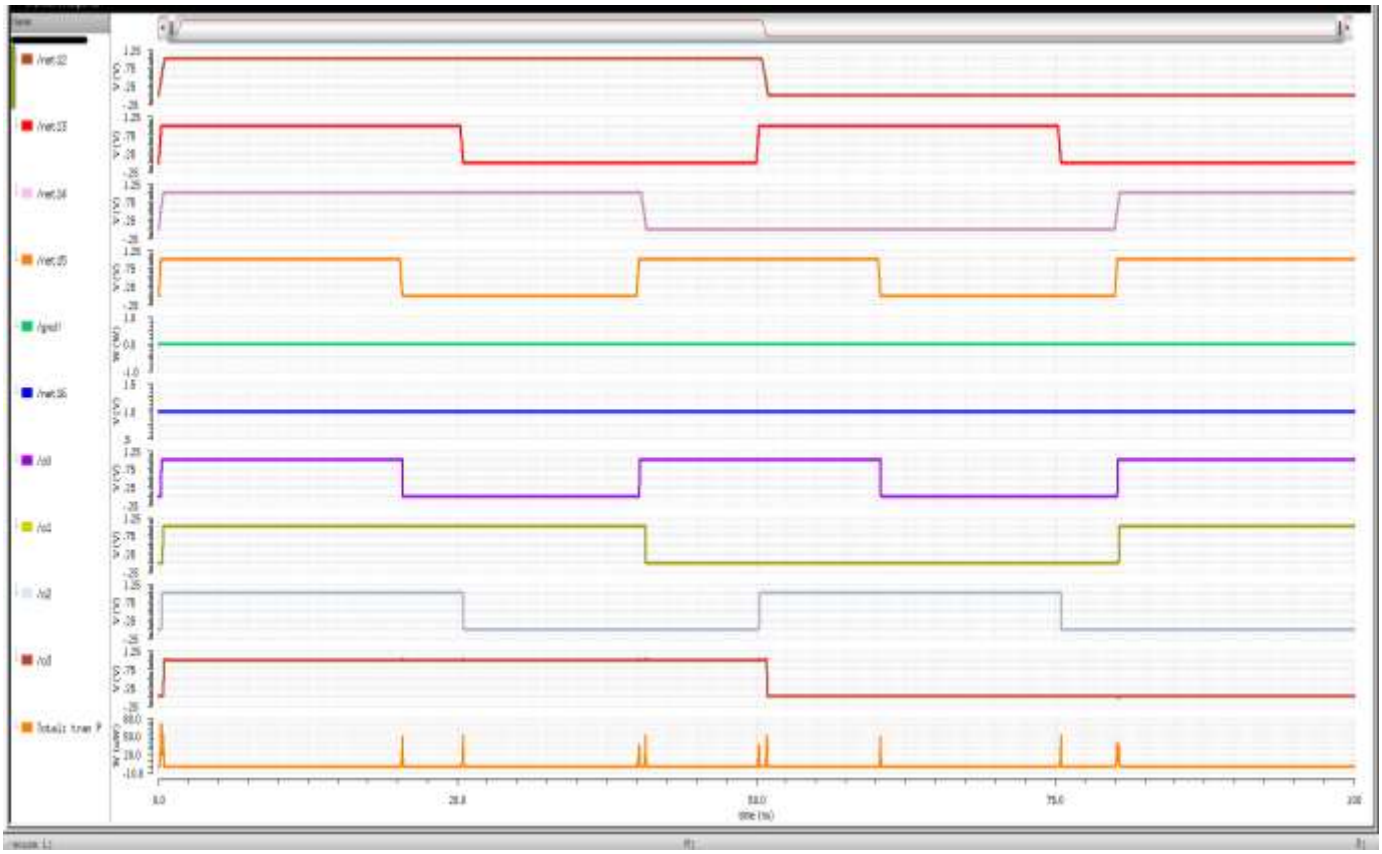


Figure 7 shows a barrel shifter, consisting of 4 input bits and three control bits. The control bits decide number of shifts from 0, 1, 4 shifts respectively.

5. Conclusion

All the designs mentioned are designed in cadence virtuoso 45nm technology. These circuits are simulated for given inputs and its transient response are reported. The delay and power are reported in table 2. Also, the comparison of DSP blocks in terms of power and delay are shown in the Figure 8 and Figure 9 respectively.

Table II- Comparison of Power and Delay of DSP Blocks in CMOS and using Modified GDI Technique

Design	CMOS		Modified GDI	
	Power (in µW)	Delay (in ps)	Power (in µW)	Delay (in ps)
KSA	1.98	11.09	1.47	3.408
Braun Multiplier with KSA	12.16	241	9.453	229.5
Barrel Shifter	0.4007	209.8	0.396	173.4

Fig. 8- Power Repot

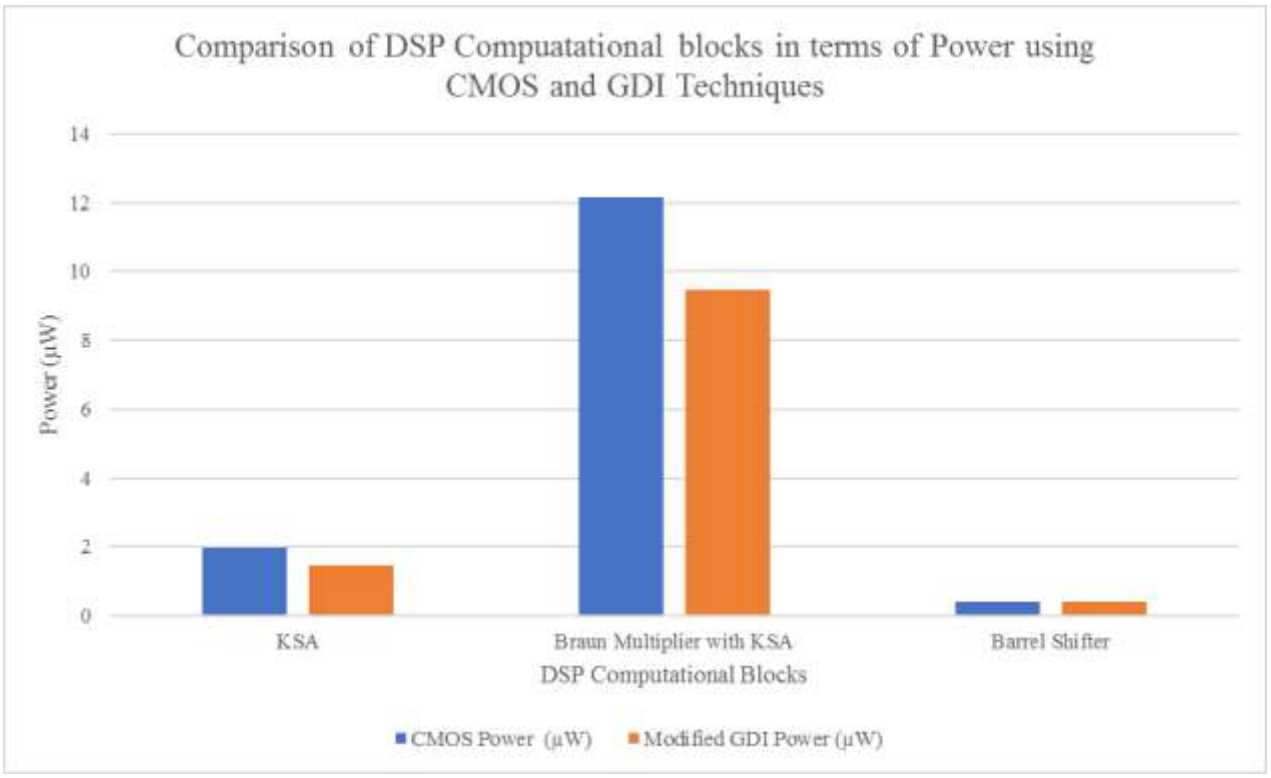
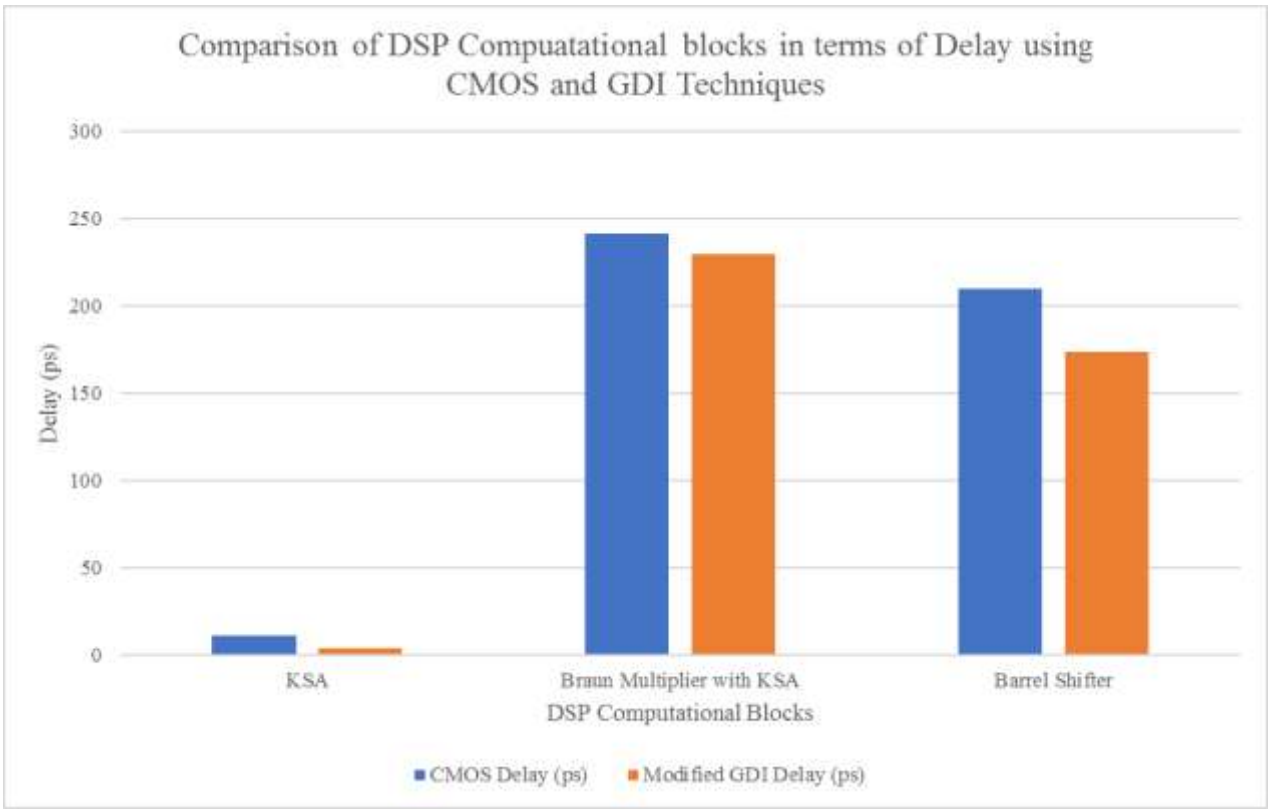


Fig. 9- Delay Report



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Kogge stone adder using modified GDI technique reduces delay by 25% and power by 69%. Braun Multiplier with KSA using GDI reduces 22% delay and 5% power. For Barrel shifter, delay and power are reduced by 1.1% and 17% respectively.

These give the chance to design separate ICs for individual blocks. Further power reduction can be achieved by designing in high level technologies and other sophisticated techniques.

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