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Design of Angle based 27-level Trinary Ladder Inverter Using Cross Compiler

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Abstract
This paper presents the design of the Multi-Level Inverter circuit based on the switched ladder topology using the angle events for the level changes. The change of events for the inverter is formulated using the Half Height Algorithm. The VHDL code is utilized for the generation of the angles as digital equivalence with the resolution of 2^7 bits. In ladder topology, there are several types of inverter namely Binary Ladder Inverter, Ye Progression, Luo Progression. Among all these topologies, the Trinary Ladder topology is advantageous for the number of levels attainment with the less number of switches. Also, the carrier-based modulation is erroneous with the High THD% and low Voltage Parameter values. The use of the non-carrier half-height method manipulates the accurate angle to measure acceptable THD %. The proposed Trinary Switched Ladder Inverter is cross-compiled with Xilinx Vivado and Matlab Simulink Took to evaluate the parameters such as THD%, VRMS, VPEAK, for the 27-level. The parametric analysis exhibits improvement in the proposed Ladder topology with cost, size, and performance when synthesized using the Xilinx Vivado tool.

Key-words: Tinary Ladder Inverter, Angle Method, HDL Coding, Cross-compiling.

1. Introduction

Multi-Level Inverter circuits are converters that modify the DC voltage into AC voltage. The MLI circuits are classified based on the topology and on the modulation scheme used. The modulation scheme-based Inverters are out of research scope due to the advent of new topology in the

MLI design. The advent of H-bridge circuits paid the way for high levels of AC voltage output using a very less number of switches and devices in the inverter topology.

The switching of the Inverters was symmetrical with the positive and negative cycles of the AC output. Low cost and high efficiency with acceptable component count are the main reasons for the MLI topology requirement [1]. Several methods of classification are available for the inverter, but the division of inverter topology based on switches is considered [2]. Several load-changing applications are flexible with the inverter topology of fewer switches and sources[3]. By using fewer components, the low voltage-based inverter circuit can be developed [4]. The solar-based application works at both symmetric and asymmetric modes with the two sources fed MLI circuitry [5].

The step-like output is produced with minimum %THD with the use of desirable switching devices [6] The ladder model-based inverter can adjust to several voltage values of the DC sources and switches [7]. The %THD value is low for the ladder-fed MLI with sliding transitions in the levels [8]. The HHM-SAM exhibits low %THD for any resolution of the MLI switching circuits [9]. The MLI switching controlled using the FPGA proves to be advantageous with low design complexity, high speed, adaptability, and fewer devices [10].

In this work, the Trinary Ladder Inverter topology is utilized for the validation of the 27-level AC outputs. The Digital PWM signals are produced from the angle method to change the levels as per the requirement of the Trinary Ladder Inverter circuitry. This paper explains the topology used for the evaluation of the 27-Level TLI preceded by the Angle calculation using the formulation and then the cross-compiling of the VHDL code in the MATLAB SIMULINK tool.

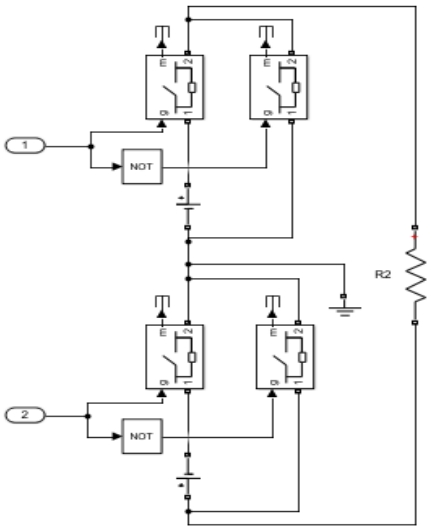
2. The Proposed 27-Level Trinary Ladder Inverter

The proposed work includes the design of a 27-level Trinary Ladder MLI circuit using the non-carrier-based angle method. The 27-level Angle-based Trinary Ladder inverter is developed using the VHDL code and validated for its operation using the cross-compiling of the HDL code into the MATLAB SIMULINK model. The cross-compiling of the proposed 27-level TLI provides the advantage of connecting the HDL code for validation with the analog circuitry of the proposed TLI. This section discusses the Trinary Ladder Inverter topology, angle calculation for the 27-level TLI, and HDL code for the proposed 27-level TLI.

a) Trinary Ladder Inverter

The Switched Ladder topology defines the arrangement of MOSFET switches in the form of a vertical ladder structure as shown in Fig.1. The Switched Ladder topology of Multi-level Inverter is divided into two parts namely positive wing and negative wing. The positive wing of the switched ladder circuit consists of the forward direction of the voltages (i.e., above the ground terminal of the ladder structure). The negative wing of the ladder circuit includes the reverse direction of the voltages (i.e., below the ground terminal of the ladder topology). The switches in the proposed ladder topology are ON and OFF according to the level requirement of the MLI.

Fig. 1 - Switched Ladder Multi-Level Inverter Circuit Using MATLAB Simulink Tool



The TLI utilizes the Trinary progression for the DC source in the ladder structure. The voltage sources are assigned with Trinary progression values such as 3^0 = 1V, 3^1 = 3V, 3^2 = 9V, 3^3=27V and so on. The formulation for the DC voltage sources of the TSLI circuit is given by

$$V_{DCN} = 3^N E \quad (1)$$

Where N = number of Levels

E = voltage

b) Non-carrier Angle based Digital PWM Signal Generation

The MLI circuits are based on the carrier-based modulation technique for the generation of the PWM signals. Depending on the number of levels in the MLI, the carrier count is fixed. The

orientation of the carrier signals decides the modulation schemes namely as Phase Disposition, Phase Opposite Disposition, and Alternate Phase Opposite Disposition, etc. The carrier-based modulation schemes for the generation of the PWM signals are inaccurate and thus increase the %THD of the AC output of the Inverter. To overcome this, the non-carrier-based DPWM signal generation is preferred for its accuracy and ease in design. The angle-based manipulation for the MLI includes the use of a mathematical formulation for the accurate evaluation of the events. The mathematical formula used in this work is given in equation (2).

$$\alpha_i = \sin^{-1}\left[\left(i - \frac{1}{2}\right)\frac{2}{N-1}\right] = \sin^{-1}\left(\frac{2i-1}{N-1}\right) \qquad (2)$$

$$where\ i = 1,2,\ldots.,\frac{N-1}{2}$$

The formulation calculates the number of angles to be utilized for the given level of the MLI circuit. Although the other angle formulations are available, the Half Height Angle calculation is more precise and thus it is used for the design of the proposed 27-level TLI.

c) 27-level Trinary Ladder Multi-Level Inverter

The Angle Algorithm is utilized for the generation of the 27-level TLI AC output. The HH-SAM for the 27-level TLI includes 13-levels in both the positive and negative cycle and a zero level. The 13 DPWM signals for the positive cycle are generated based on the switching angles for the ON and OFF states. For a quadrant, there are 13 angles generated for the ON of the 13 DPWM signals and another 13 angles are generated for the OFF of the 13 DPWM signals for the positive cycle of the AC MLI output. Similarly, for the negative cycle, there are 26 angles generated and thus the proposed 27 TLI methods consist of 42 angles for one cycle of the AC output. To represent the generated 42 angles in digital, the AC output of one cycle is equated to desired bit resolution. In this work, the maximum angle for one cycle AC output is 360 is equated to the 2^7-bit value (i.e., 128). Thus the quadrants are represented as given in Table 1.

Table 1 - Bit Equivalence for the Quadrants Angles of the Multi-Level Inverter

Quadrant	**Angles**	**2^7 Bit resolution**
First	0 – 90	0 – 32
Second	90 – 180	32 – 64
Third	180 – 270	64 – 96
Fourth	270 – 360	96 – 128

The 42 angles are converted to the 2^7 bits equivalent by multiplying the scale value of 2.8125. Also, the resultant value is rounded up to the nearest integer value for coding purposes. The generated 26 DPWM signals are logically combined to derive the desired switch patterns for the 6 switches of the TLI. The Trinary Ladder Inverter requires 6 distinct switch patterns for the generation 27-level AC output.

The angle-based calculation for the 27-level TLI involves four-quadrant evaluations for the event identification of the levels. Table 2 shows the evaluation of the 13 angles of the first quadrant with the 27-bit resolution equivalent of the binary representation. The roundup method is used to derive the exact integer value of the angles. The second quadrant derivation for the 13 angles is evaluated using the 180-first quadrant angles and its binary equivalent is derived as given in Table 3. Tables 3 and 4 depict the 27-bit resolution equivalent for the negative cycle angles of the proposed 27-Level TLI.

Table 2 - First Quadrant Angles for the 27-level TLI with 27-bit Resolution

FIRST QUADRANT (0 TO 90)					
ALPHA	**2i-1**	**(2i-1/m-1)**	**SIN `1**	**128 BIT EQUAL**	**ROUNDED**
1	1	0.0384615	2.204227504	0.783725335	**1**
2	3	0.1153846	6.625809565	2.355843401	**3**
3	5	0.1923077	11.08748921	3.942218386	**4**
4	7	0.2692308	15.61849828	5.553243831	**6**
5	9	0.3461538	20.25224674	7.200798842	**8**
6	11	0.4230769	25.02899949	8.899199818	**9**
7	13	0.5	30	10.66666667	**11**
8	15	0.5769231	35.23441798	12.52779306	**13**
9	17	0.6538462	40.83221703	14.51812161	**15**
10	19	0.7307692	46.9509202	16.69366052	**17**
11	21	0.8076923	53.87107253	19.15415912	**20**
12	23	0.8846154	62.2042275	22.11705867	**23**
13	25	0.9615385	74.05763139	26.33160227	**27**

Table 3 - Second Quadrant Angles for the 27-level TLI with 27 Bit Resolution

SECOND QUADRANT (90 TO 180)						
ALPHA	**2i-1**	**(2i-1/m-1)**	**SIN `1**	**180-SIN`1**	**128 BIT EQUAL**	**ROUNDED**
13	25	0.9615385	74.05763139	105.9423686	37.66839773	**37**
12	23	0.8846154	62.2042275	117.7957725	41.88294133	**41**
11	21	0.8076923	53.87107253	126.1289275	44.84584088	**44**
10	19	0.7307692	46.9509202	133.0490798	47.30633948	**47**
9	17	0.6538462	40.83221703	139.167783	49.48187839	**49**
8	15	0.5769231	35.23441798	144.765582	51.47220694	**51**
7	13	0.5	30	150	53.33333333	**53**
6	11	0.4230769	25.02899949	154.9710005	55.10080018	**55**
5	9	0.3461538	20.25224674	159.7477533	56.79920116	**56**
4	7	0.2692308	15.61849828	164.3815017	58.44675617	**58**
3	5	0.1923077	11.08748921	168.9125108	60.05778161	**60**
2	3	0.1153846	6.625809565	173.3741904	61.6441566	**61**
1	1	0.0384615	2.204227504	177.7957725	63.21627467	**63**

Based on the calculated values of the 26 angles, the topology for the 27-level TLI is connected as shown in Fig. 2. The digital Pulse Width Modulation signals are produced by the angles from the tables. The 26 DPWM signals are logically connected to generate the switching patterns for the 6 switches of the 27-level TLI.

Table 4 - Third Quadrant Angles for the 27-level TLI with 27-bit Resolution

THIRD QUADRANT (180 TO 270)				
ALPHA	**SIN `1**	**180+SIN`1**	**128 BIT EQUAL**	**ROUNDED**
1	2.204227504	182.2042275	64.78372533	**65**
2	6.625809565	186.6258096	66.3558434	**67**
3	11.08748921	191.0874892	67.94221839	**68**
4	15.61849828	195.6184983	69.55324383	**70**
5	20.25224674	200.2522467	71.20079884	**72**
6	25.02899949	205.0289995	72.89919982	**73**
7	30	210	74.66666667	**75**
8	35.23441798	215.234418	76.52779306	**77**
9	40.83221703	220.832217	78.51812161	**79**
10	46.9509202	226.9509202	80.69366052	**81**
11	53.87107253	233.8710725	83.15415912	**84**
12	62.2042275	242.2042275	86.11705867	**87**
13	74.05763139	254.0576314	90.33160227	**91**

Table 5 - Fourth Quadrant Angles for the 27-level TLI with 27-bit Resolution

FOURTH QUADRANT(270 TO 360)				
ALPHA	**SIN `1**	**360-SIN`1**	**128 BIT EQUAL**	**ROUNDED**
13	74.05763139	285.9423686	101.6683977	**101**
12	62.2042275	297.7957725	105.8829413	**105**
11	53.87107253	306.1289275	108.8458409	**108**
10	46.9509202	313.0490798	111.3063395	**111**
9	40.83221703	319.167783	113.4818784	**113**
8	35.23441798	324.765582	115.4722069	**115**
7	30	330	117.3333333	**117**
6	25.02899949	334.9710005	119.1008002	**119**
5	20.25224674	339.7477533	120.7992012	**120**
4	15.61849828	344.3815017	122.4467562	**122**
3	11.08748921	348.9125108	124.0577816	**124**
2	6.625809565	353.3741904	125.6441566	**125**
1	2.204227504	357.7957725	127.2162747	**127**

Fig. 2 - Schematic Diagram for the 27-level Trinary Ladder Inverter Topology

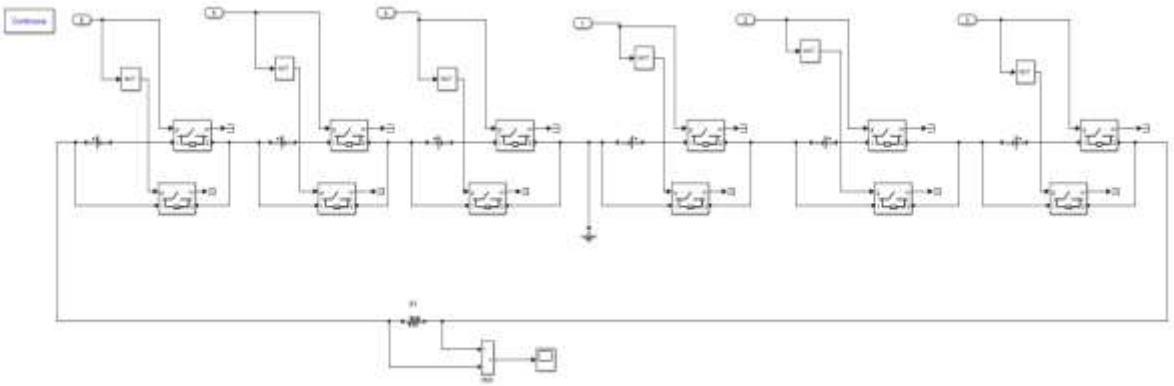


Table 6 - Voltage Combination for the Positive Levels and Negative Levels of the 27-level TLI

Positive Levels	Voltage Combinations	Negative Levels	Voltage Combinations
13	+1+3+9	-13	-1-3-9
12	+3+9	-12	-3-9
11	-1+3+9	-11	+1-3-9
10	+1+9	-10	-1-9
9	+9	-9	-9
8	-1+9	-8	+1-9
7	+1-3+9	-7	-1+3-9
6	-3+9	-6	+3-9
5	-1-3+9	-5	+1+3-9
4	+1+3	-4	-1-3
3	+3	-3	-3
2	-1+3	-2	+1-3
1	+1	-1	-1
0	0	0	0

The switching pattern for the 6 switches is based on the voltage combination of the 27 levels is given in Table 6. The voltage levels combinations for the positive levels and negative levels of the 27 levels TLI assure the corresponding voltage sources to be utilized in sequence. The switching control of 6 switches for the 27-level TLI is based on the pattern given in Tables 7 and 8. Table 7 shows the positive level switching pattern for the six switches with the 1's and 0's represented as ON and OFF respectively based on the levels of the TLI. Table 8 represents the switching control for the six switches for the negative level of the proposed 27-level TLI. The pattern of each switch is consolidated to form the switch pattern of the proposed method. This work concentrates on the generation of these 6 switch patterns using the synthesizable VHDL code and validated using the cross-compiling in MATLAB SIMULINK block.

Table 7 - Positive Level Switch Pattern for the 27-level Trinary Ladder Inverter

Levels	S1	S3	S9	S1B	S3B	S9B
13	1	1	1	0	0	0
12	0	1	1	0	0	0
11	0	1	1	1	0	0
10	1	0	1	0	0	0
9	0	0	1	0	0	0
8	0	0	1	1	0	0
7	1	0	1	0	1	0
6	0	0	1	0	1	0
5	0	0	1	1	1	0
4	1	1	0	0	0	0
3	0	1	0	0	0	0
2	0	1	0	1	0	0
1	1	0	0	0	0	0
0	0	0	0	0	0	0

Table 8 - Negative Level Switch Pattern for the 27-level Trinary Ladder Inverter

Levels	S1	S3	S9	S1B	S3B	S9B
-13	0	0	0	1	1	1
-12	0	0	0	0	1	1
-11	1	0	0	0	1	1
-10	0	0	0	1	0	1
-9	0	0	0	0	0	1
-8	1	0	0	0	0	1
-7	0	1	0	1	0	1
-6	0	1	0	0	0	1
-5	1	1	0	0	0	1
-4	0	0	0	1	1	0
-3	0	0	0	0	1	0
-2	1	0	0	0	1	0
-1	0	0	0	1	0	0
0	0	0	0	0	0	0

3. Results and Discussions

The 27-level TLI is designed as per the angle method for triggering the level changes. As discussed the number of DPWM signals generated for the 27 levels is 13 each at the positive and

negative levels with a zero level. The DPWM signal is logically combined to produce the required Switch patterns for the 6 switches of the Trinary ladder MLI. The 26 DPWM signals are generated by the angle method manipulation as shown in Fig.3. Fig.4 depicts the switch patterns for the 6 switches of the Trinary Ladder MLI circuit.

Fig 5 shows the 6 switch patterns generated using the cross-compiling of the developed VHDL code into MATLAB SIMULINK block. The system generator tool is utilized for the conversion of the HDL code to the SIMULINK block. The generated 6 switch patterns are fed to the analog TLI circuit to produce the AC output as depicted in Fig. 6. In Fig.7, the 27 level TLI consists of 13-levels in the positive cycle and 13-levels in the negative cycle. The %THD for the proposed 27-level TLI is simulated using the MATLAB SIMULINK Tool with 3.52% and VPEAK as 128.2 V. The parametric evaluation for the proposed method is shown in Fig.8 with the VRMS as 90.64. The developed HDL code for the 27-level TLI is synthesized using the Xilinx VIVADO tool as represented in Fig. 9. Also, the power analysis is derived using the Xilinx VIVADO tool for the evaluation of Dynamic power as 1.565W and Static power as 0.097W as shown in Fig 10. The device utilization chart for the proposed method is given in Table 9 and proves to be advantage for low usage of components.

Fig. 3 - Simulation for the 26 Digital PWM based on angle Method for the 27-level TLI Using ModelSim Software Tool

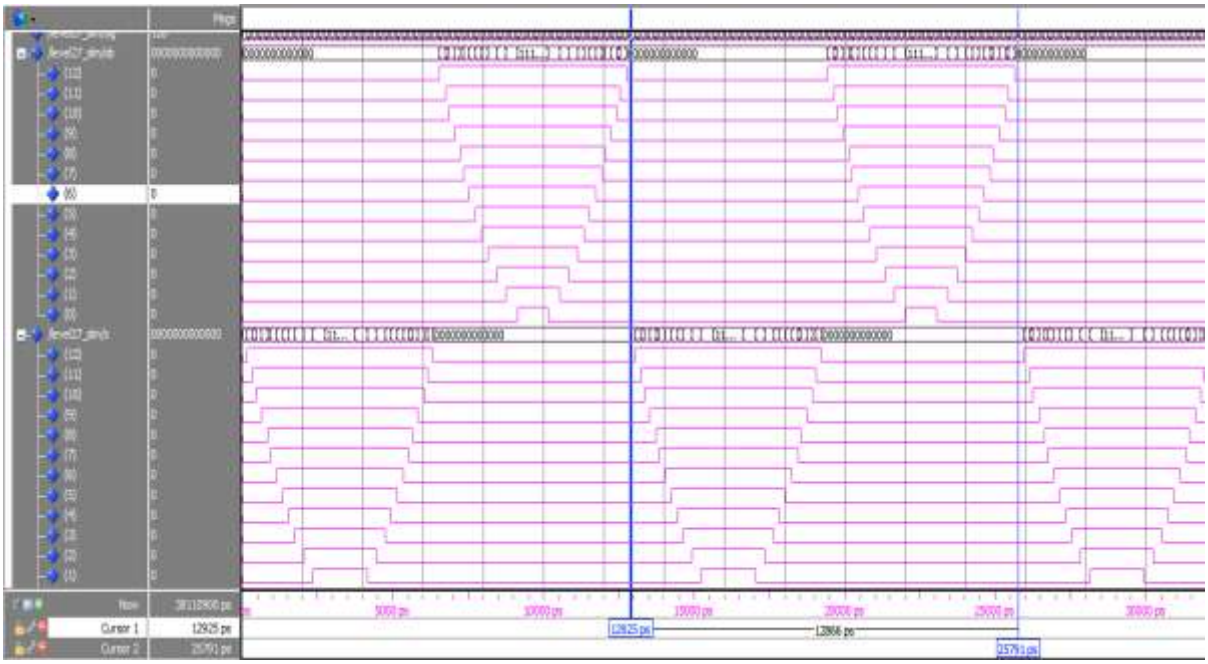


Fig. 4 - Simulation for the 6 Switching Patterns for the 27-level TLI Using ModelSim Software Tool

Fig. 5 - Simulation of the 6 Switching Pattern for the 27-level TLI Using Cross-compiling

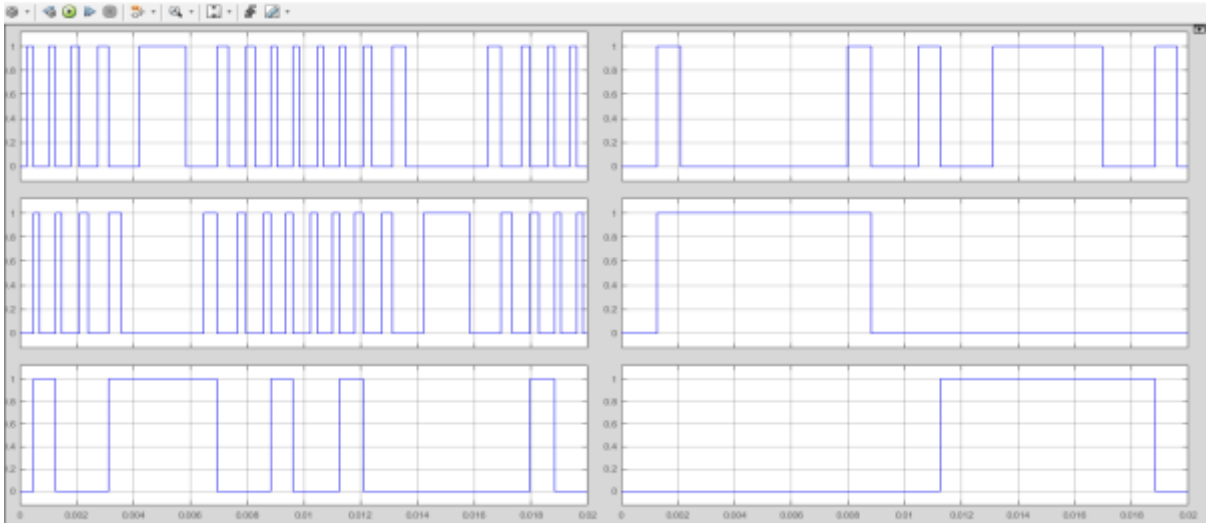


Fig. 6 - AC Inverter Output for the Proposed 27-level TLI Using the Cross-compiling

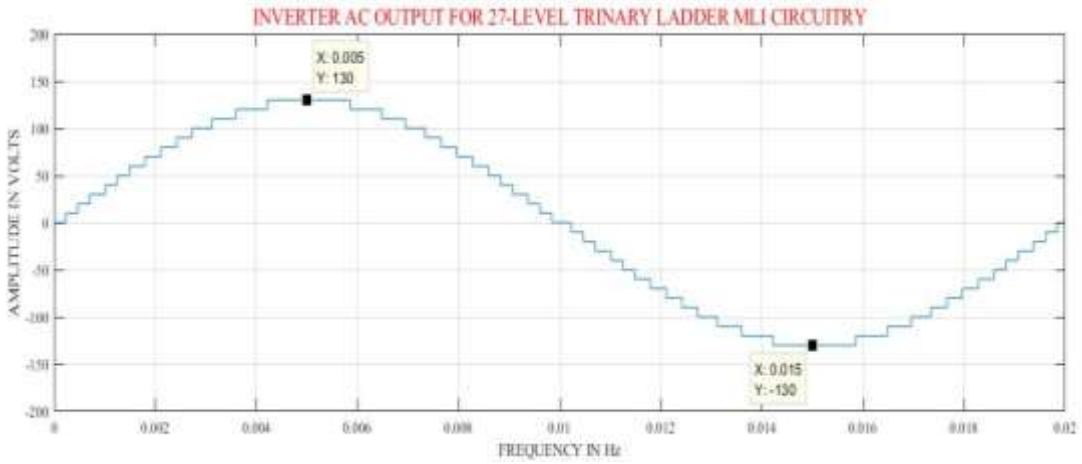


Fig. 7 - Simulation Evaluation of the %THD Parameter for the Proposed 27-level TLI

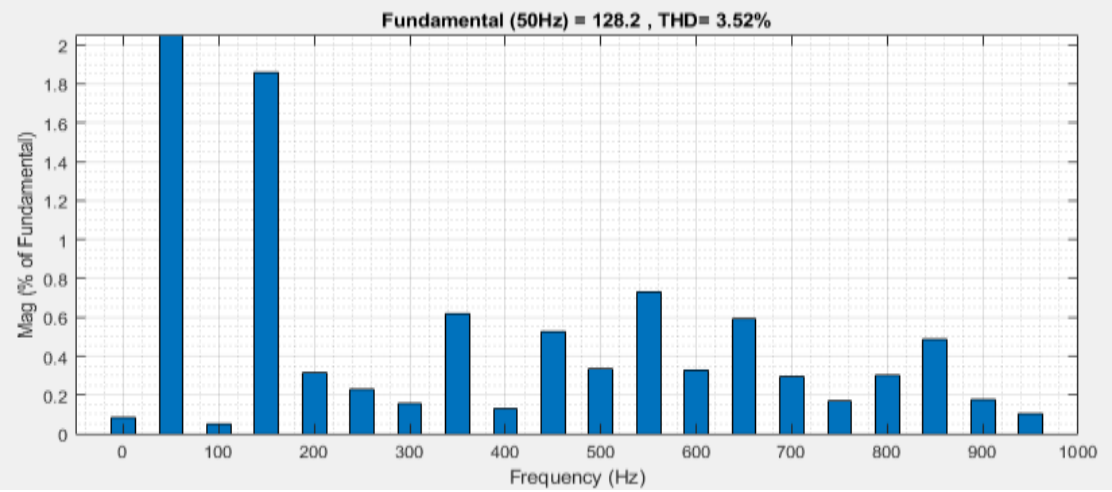
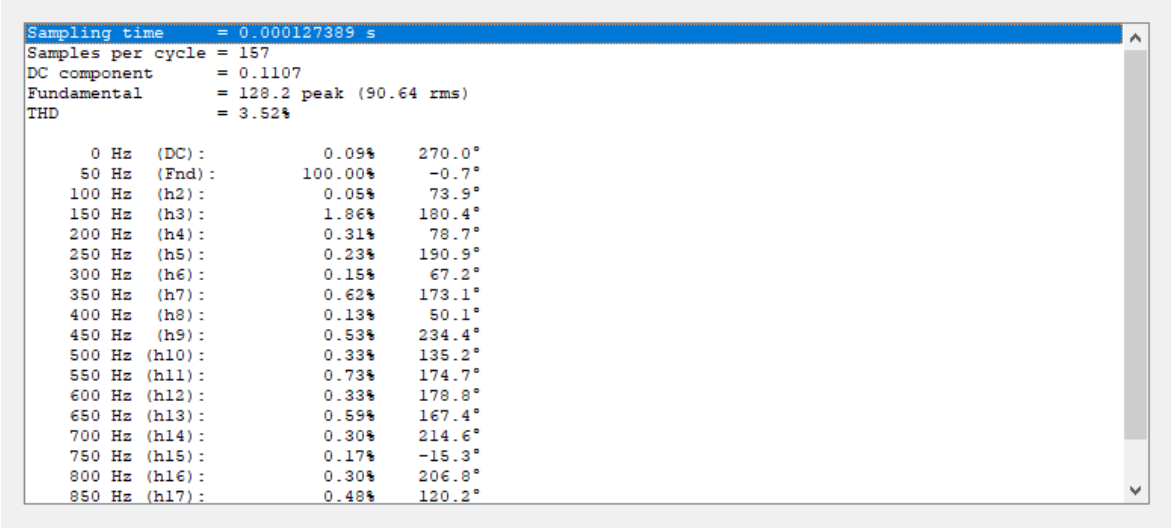


Fig. 8 - Simulation Evaluation of the V_{RMS}, V_{PEAK} Parameters for the Proposed 27-level TLI



```
Sampling time     = 0.000127389 s
Samples per cycle = 157
DC component      = 0.1107
Fundamental       = 128.2 peak (90.64 rms)
THD               = 3.52%

     0 Hz   (DC):          0.09%    270.0°
    50 Hz   (Fnd):       100.00%     -0.7°
   100 Hz   (h2):          0.05%     73.9°
   150 Hz   (h3):          1.86%    180.4°
   200 Hz   (h4):          0.31%     78.7°
   250 Hz   (h5):          0.23%    190.9°
   300 Hz   (h6):          0.15%     67.2°
   350 Hz   (h7):          0.62%    173.1°
   400 Hz   (h8):          0.13%     50.1°
   450 Hz   (h9):          0.53%    234.4°
   500 Hz   (h10):         0.33%    135.2°
   550 Hz   (h11):         0.73%    174.7°
   600 Hz   (h12):         0.33%    178.8°
   650 Hz   (h13):         0.59%    167.4°
   700 Hz   (h14):         0.30%    214.6°
   750 Hz   (h15):         0.17%    -15.3°
   800 Hz   (h16):         0.30%    206.8°
   850 Hz   (h17):         0.48%    120.2°
```

Fig. 9 - Schematic design flow for the developed VHDL code of the proposed 27-level TLI

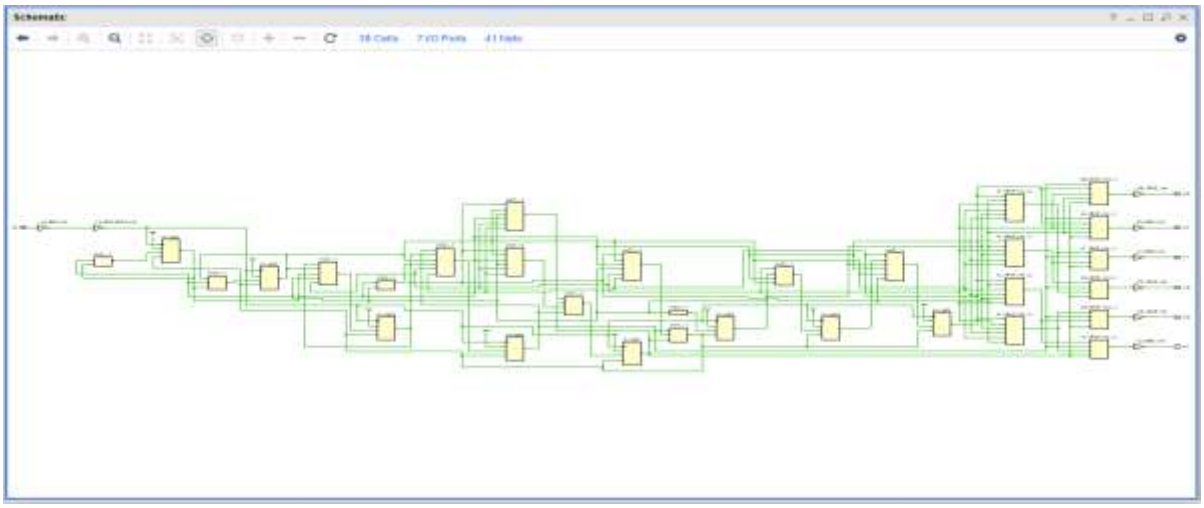


Fig. 10 - Power Analysis Report for the Proposed 27-level TLI Using the XILINX VIVADO Tool

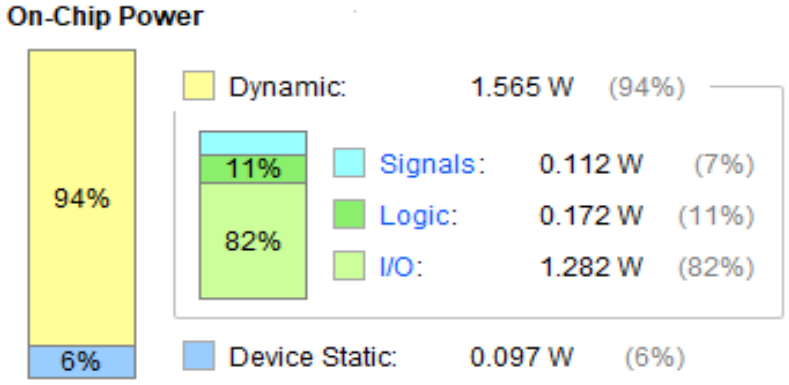


Table 9 - Device Utilization Chart for the Proposed 27-level TLI Using the XILINX VIVADO Tool

Resource	Utilization	Available	Utilization ...
LUT	17	63400	0.03
FF	8	126800	0.01
IO	7	210	3.33
BUFG	1	32	3.13

4. Conclusion

The proposed 27 levels Trinary Ladder Inverter was successfully developed using the HDL code. The validation of the 27-level TLI circuit is attained by the cross-compiling of HDL code with the MATLAB SIMULINK tool. The performance analysis for the inverter was evaluated for %THD, Vpeak, Vrms, and Power. The % THD for the proposed inverter was 3.52% with the Vrms = 90.64V and Vpeak = 128.2 V. The developed VHDL code was synthesized using the Xilinx VIVADO tool to achieve low dynamic power dissipation of 1.565W and with low utilization of device for the FPGA device. The improvement in the levels of the proposed ladder-type inverter could be considered for the future extension of the work.

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